Code No: R201221 **R20** SET - 1

I B. Tech II Semester Regular/Supplementary Examinations, August- 2022

DIGITAL LOGIC DESIGN

(CSE-CS&T, CSE-AI&ML, CSE-AI, CSE-DS, CSE-AI&DS, CSE-CS, CSE-IOT&CS INCL BCT, CSE-CS&BS,CSE-IOT, AI&DS, Cyber Security)

Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1 a) Convert the following (9M)
   i) 110001.1010010 into hexadecimal
   ii) $(AB)_{16} = (\ )_{10}$
   iii) $(1234)_8 = (\ )_2$

   b) Explain the BCD, Excess 3, alphanumeric codes with examples. (5M)

Or

2 a) Represent the decimal number 4608 in (6M)
   i) BCD ii) Excess-3 code.

   b) Perform (-20)-(-10) in binary using the signed-2's complement and 1's complement. (8M)

UNIT-II

3 a) Simplify the Boolean expressions to minimum number of literals (7M)
   i) A+B+A'B'C
   ii) AB + A (B +C) + B'(B+D)

   b) Simplify the Boolean expression using K-MAP (7M)
   $F(A,B,C,D) = \pi\ (3,5,6,7,11,13,14,15) + d(9,10,12)$

Or

4 a) Reduce the expression $f(x,y,z,w) = \pi(0,2,7,8,9,10,11,15) + d\ (3,4)$ using K-Map. (7M)

   b) Prove that the sum of all minterms of Boolean function for three variables is 1. (7M)

UNIT-III

5 a) Design a binary full adder with two half adders and basic gates. (7M)

   b) Given 32 × 8 ROM with enable input, Show the external connections necessary to construct a 128 × 8 ROM with 4 chips and a decoder. (7M)

Or

6 a) Write the functions of a decoder and multiplexer. (7M)

   b) Write the HDL model of a 4:16 decoder. (7M)
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UNIT-IV

7 a) Explain the Logic diagram of JK flip-flop? Draw the Truth table and Excitation Table. (7M)

b) Convert a D flip flop into SR flip flop. (7M)

Or

8 a) Write the differences between Combinational & Sequential circuits. (7M)

b) Convert a T flip flop to D flip flop. (7M)

UNIT-V

9 a) Explain synchronous and ripple counters compare their merits and demerits. (7M)

b) With neat sketch explain a 4-bit bidirectional shift register. (7M)

Or

10 a) Design a modulo -13 up synchronous counter using SR- flip flops and draw circuit diagram. (7M)

b) Explain a 4- bit left shift register with JK flip flops. (7M)

Code No: R201221 **R20** SET - 2

I B. Tech II Semester Regular/Supplementary Examinations, August- 2022

DIGITAL LOGIC DESIGN

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Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1 a) Convert the following numbers. (9M)
   i) (423.25)10 into Hexadecimal.
   ii) (11001101.0101)2 to base-8 and base-4

   b) Represent the decimal number 8620 in i) BCD ii) Excess-3 code. (5M)

Or

2 a) Determine the value of base x if$(211)_x=(152)_8$. (5M)

   b) Perform binary subtraction using 1's & 2's complement methods. (9M)

UNIT-II

3 a) Implement the Boolean function F(A,B,C,D)= A'B'+C'D'+B'C' using two input NAND gates and NOR gates only. (7M)

   b) Convert the following to canonical forms (7M)
   i) $F(x,y,z,w)=\sum(1,3,7,9,11,12)$ ii) $F(A,B,C) = \pi (0,3,6,7)$

Or

4 a) Simplify the Boolean function using K-map method. (7M)
   $F=\sum(1,3,4,5,10,11,12,13,14,15)$.

   b) Derive and Implement Exclusive OR function involving three variables using only NAND function (7M)

UNIT-III

5 a) Construct the PROM using the conversion from BCD code to Excess-3 code. (7M)

   b) Implement 4x16 decoder using two 3x8 decoders. (7M)

Or

6 a) Explain about Priority Encoder. (7M)

   b) Design PAL for a combinational circuit that squares a 3 bit number. (7M)

UNIT-IV

7 a) What is race-around condition? How does it eliminated in Master –slave J-K flip-flop? (7M)

   b) How do you convert one type of flip-flop into another? Explain with an Example. (7M)
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Or

8 a) Write the differences between latches and flip flops? Write the truth table of clocked JK- Flip Flop? (7M)

b) Realize D-latch using S-R latch. (7M)

UNIT-V

9 a) What is a register? What are the different classifications of Shift Registers? Discuss the applications of shift registers? (7M)

b) Design and draw the 3 bit up-down synchronous counter? (7M)

Or

10 a) Draw the logic diagram for a 4-bit binary ripple counter using positive edge triggered JK flip-flops (7M)

b) Explain a right shift register with an example. (7M)

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I B. Tech II Semester Regular/Supplementary Examinations, August- 2022

DIGITAL LOGIC DESIGN

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Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1 a) What is the use of complements? Perform subtraction using 9's complement for the given numbers i. (565)-(666) ii. (763) –(567) (5M)

b) Convert the following numbers (9M)
i) (41.6875)10 =( )16
ii) (4567)10 =( )2
iii) (101110.01)2=( )8

Or

2 a) Subtract the following using 1's and 2's complement (101)2 - (10110)2. (5M)

b) Convert the following (9M)
i) 110001.1010010 in to decimal.
ii) Convert $(423.25)_{10}$ into Hex.
iii) $(7\ A\ 69)_{16}$ into decimal

UNIT-II

3 a) Obtain the simplified expression in SOP form of F(a,b,c,d,e)=∑(1,2,4,7,12,14,15,24,27,29,30,31)using K-maps. (7M)

b) Simplify the following expression using Boolean algebra rules (7M)

$$\overline{A\bar{B} + ABC + A(B + A\bar{B})}$$

Or

4 a) simplify the Boolean expression using K-MAP (7M)
F(A,B,C,D) = ∑m(1,2,3,8,9,10,11,14) +d(7,15)

b) Implement the function f(a,b,c)=π(0,1,3,4) using NAND-NAND two level gate structure (7M)

UNIT-III

5 a) Design the combinational circuit of Binary to Excess-3 code convertors? (7M)

b) Implement the following Boolean functions using PLA with 3 AND gates. (7M)
F1 (ABC) = ∑ (3,5,7), F2 = ∑(4,5,7)

Or

6 a) Discuss about HDL Models of Combinational Circuits (7M)

b) Implement the following Boolean function using 8:1 multiplexer (7M)
F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD

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UNIT-IV

7 a) Define Flip-flop and various types of flip flops? Explain the working of S- R flip-flop Using NAND Gate. (7M)

b) Convert an JK Flip-Flop into D Flip-Flop. (7M)

Or

8 a) Draw and explain the operation of D Flip-Flop? Draw the Truth and Excitation Tables (7M)

b) Convert an SR Flip-Flop into T Flip-Flop. (7M)

UNIT-V

9 a) What is the function of shift register? With the help of simple diagram explain its working. (7M)

b) Design 4 bit binary synchronous counter Using JK-flip flop. (7M)

Or

10 a) Design and explain Johnson counter. (7M)

b) Explain the working of SIPO shift register with logic diagram and waveforms (7M)

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Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1 a) Convert the following (9M)
i. $(BA69)_{16}$ to base 2, base 4, and base 8.

b) Subtract $(111001)_2$ from (101011) using 1's complement? (5M)

Or

2 a) Convert the following (7M)
i) $(657)_8$ into decimal.
ii) Convert $(2348)_{10}$ into hexa decimal

b) Add (+48) and (-27) using 2′s complement. (7M)

UNIT-II

3 a) Simplify the Boolean expressions to minimum number of literals (7M)
i) AB + (AC)' + AB'C(AB + C)
ii) (A+B)' (A'+B')'

b) Convert the given expression in standard POS and SOP forms Y= A.(A+B+C) (7M)

Or

4 a) Simplify the Boolean expression using K-map and implement using NOR gates (7M)
F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14).

b) Obtain the simplified expression in sum of products for the following Boolean function. (7M)
a) F(A,B,C,D) = ∑(2,3,12,13,14,15).
b) BDE+B′C′D+CDE+A′B′CE+A′B′C+B′C′D′E′

UNIT-III

5 a) Design a 4 bit magnitude comparator (7M)

b) Implement the following functions using PLA. A(x,y,z) = ∑m(1,2,4,6) B(x,y,z) = ∑m(0,1,6,7) c(x,y,z) = ∑m(2,6) (7M)

Or

6 a) Design a 4 bit adder-subtractor circuit and explain the operation in detail. (7M)

b) Define a multiplexer? Draw a 4:1 multiplexer for the function f(a,b,c,d)=∑(0, 4,5,10,11,12,15) (7M)
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UNIT-IV

7	a)	Draw and explain the operation of T Flip-Flop? Draw the Truth and Excitation Tables.	(7M)
	b)	Convert an SR Flip-Flop into JK Flip-Flop.	(7M)

Or

8	a)	Explain about a NOR Latch in detail, with a neat diagram.	(7M)
	b)	Convert an T Flip-Flop into JK Flip-Flop.	(7M)

UNIT-

9	a)	Explain the design of a 4 bit binary counter with parallel load in detail?	(7M)
	b)	Explain about Ring counter.	(7M)

Or

10	a)	Design 5 -bit counter using D flip flops.	(7M)
	b)	With a neat diagram explain about Universal shift register.	(7M)