Code No: **R201221** **R20** **SET - 1**

I B. Tech II Semester Supplementary Examinations, January/February - 2023

DIGITAL LOGIC DESIGN

(Common to CSE-CS&T, CSE-AI&ML, CSE-AI, CSE-DS, CSE-AI&DS, CSE-CS, CSE-IOT&CS INCL BCT, CSE-CS&BS,CSE-IOT, AI&DS, Cyber Security)

Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT - I

1 a) Perform the following using BCD arithmetic. [7M]
i) $(79)_{10} + (177)_{10}$ ii) $(481)_{10} + (178)_{10}$

b) Perform the subtraction operation by using 2's complements [7M]
i) 11100101-101011 ii) $(12378)_{10}$-$(10230)_{10}$

(OR)

2 a) Encode the decimal number 493 in (i) Binary (ii) BCD (iii) ASCII (iv) Excess – 3. [7M]

b) Explain about the Binary Codes, BCD and 2421codes. [7M]

UNIT - II

3 a) Simplify the Boolean expressions to minimum number of literals [7M]
i) X' + XY + X Z' + XYZ' ii) (X+Y) (X+Y').

b) Implement the Boolean function F (A, B, C, D) = A'B'+C'D'+B'C' using the following two level gates i) NAND-AND ii) NOR-OR. [7M]

(OR)

4 a) Simplify the Boolean expression using K-MAP [7M]
F(A,B,C,D) = πM (3,5,6,7,11,13,14,15) +d(9,10,12)

b) Find the complement of the function and represent in sum of minterms and product of maxterms F(x,y,z) = xy + z'. [7M]

UNIT - III

5 a) Implement the function F = ∑m (0, 1, 2, 4, 5, 8, 11, 12, 15) using 8:1 multiplexer. [7M]

b) Implement the following Boolean functions using PAL. [7M]
(i) A=XY+XZ′, B=XY′ +YZ′ ii) A=XY+XZ, B=XY′+YZ+XZ.

(OR)

6 a) Construct 4*16 Decoder with help of 2*4 Decoder. [7M]

b) Implement the following functions using PLA with three inputs, four product terms and two outputs. [7M]
F1 (A, B, C) = ∑m (3, 5, 6, 7)
F2 (A, B, C) = ∑m (0, 2, 4, 7).

UNIT - IV

7 a) Draw the circuit diagram of positive edge triggered JK flip-flop with NAND gates and explain its operation using truth-table. [7M]

b) Convert RS flip flop to a i) D-latch ii) T-latch. [7M]

(OR)

8 a) Construct the D flipflop with the help of truth table and excitation table. [7M]

b) What is race-around condition? How does it set eliminate using a Master –slave J-K flip-flop? [7M]

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UNIT - V

9 a) Develop the design steps of synchronous counters with suitable examples. [7M]

b) Using D-Flip flops and wave forms, explain the working of a 4-bit SISO shift register. [7M]

(OR)

10 a) Design 5stage twisted ring counter with circuit diagram, state transition diagram and state table. [7M]

b) Design MOD -6 Ripple Down counters. [7M]

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