Code No: **R201221** **R20** **SET - 1**

I B. Tech II Semester Supplementary Examinations, Jan/Feb-2024

DIGITAL LOGIC DESIGN

(CSE-CS&T, CSE-AI&ML, CSE-AI, CSE-DS, CSE-AI&DS, CSE-CS, CSE-IOT&CS INCL BCT, CSE-CS&BS,CSE-IOT, AI&DS, Cyber Security)

Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1 a) Explain four bit codes used in the number system and give examples. [7M]

b) Perform subtraction by using 2's complement for the given [7M]
i. 111011-1010.
ii. 1100-1010110

(OR)

2 a) Perform subtraction by using 9's complement for the given: [7M]
i. 845-245.
ii. 236-673

b) Convert the following to the required form. [7M]
i) $(A98B)_{12} = ()_3$ ii) $(38.65)_{10} = ()_2$ iii) $10010011_2 = ()_{16}$

UNIT-II

3 a) Prove that the sum of all min terms of Boolean function for three variables is 1. [7M]

b) Obtain the simplified expression in POS form using K-map method and NOR gate level implementation for the following: $F(A,B,C,D)=\pi(0,4,5,7,8,9,13,15)$ [7M]

(OR)

4 a) Using K-map find the Boolean function and its complement for the following: $F(A,B,C,D) = \sum(1,2,3,4,6,8,9,10,11,12,14)$. [7M]

b) Explain with neat logic diagram and truth table of the functioning of basic logic gates. [7M]

UNIT-III

5 a) Implement the following functions using a multiplexer: [7M]
(i) $F(x,y,z) = \sum(1,2,6,7)$
(ii) $F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$

b) Design a half subtractor using logic gates. [7M]

(OR)

6 a) Explain the working of a De-multiplexer with the help of an example. [7M]

b) Realize the following four Boolean functions using PAL. [7M]
$F1(W,X,Y,Z) = \sum m(0,1,2,3,7,9,11)$
$F2(W,X,Y,Z) = \sum m(0,1,2,3,10,12,14)$
$F3(W,X,Y,Z) = \sum m(0,1,2,3,10,13,15)$
$F4(W,X,Y,Z) = \sum m(4,5,6,7,9,15)$

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UNIT-IV

7 a) What is the difference between latch and flip flop? Discuss about D-Latch and SR-Latch. [7M]

b) Convert T flip flop into JK-flip flop. Draw and explain the logic diagram. [7M]

(OR)

8 a) Give the characteristic table, Truth table, characteristic equation and excitation table for T and D Flip Flop. [7M]

b) Implement D- Flip Flop using T Flip Flop with its truth table. [7M]

UNIT-V

9 a) Explain synchronous and ripple counters compare their merits and demerits. [7M]

b) Draw and explain a 4-bit Serial in Parallel out (SIPO) Shift Register. [7M]

(OR)

10 a) Build a 4bit universal shift register using D flip flops and multiplexers. [7M]

b) Explain Johnson Counters. How it is different from other counters. [7M]

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