

**I B. Tech II Semester Regular/Supplementary Examinations, July/August - 2023****DIGITAL LOGIC DESIGN**(Common to CSE-CS&T, CSE-AI&ML, CSE-AI, CSE-DS, CSE-AI&DS, CSE-CS, CSE-IOT&CS  
INCL BCT, CSE-CS&BS, CSE-IOT, AI&DS, Cyber Security)

Time: 3 hours

Max. Marks: 70

*Answer any five Questions one Question from Each Unit  
All Questions Carry Equal Marks***UNIT-I**

- 1 a) Convert the following to Decimal and then to octal [7M]  
i)  $(125F)_{16}$  ii)  $(10111111)_2$  iii)  $(392)_{10}$   
b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property? [7M]

**(OR)**

- 2 a) With suitable examples discuss the subtraction of two numbers using radix complement and diminished radix complement forms. [7M]  
b) What is 2421 code? Write the code words for 0-9 using 2421 code? Differentiate between BCD code and 2421 code? [7M]

**UNIT-II**

- 3 a) Without reducing, implement the following expressions in AOI logic and then convert them into NAND logic and NOR logic  $A + BC + (A + B'C) + D$  ii)  $A + B'C + (B + C)' + B'C'$ . [7M]  
b) Reduce using mapping the following expression and implement the real minimal expression in Universal logic.  $F = \sum m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$ . [7M]

**(OR)**

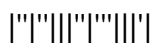
- 4 a) State and prove consensus theorem? Solve the given expression using consensus theorem. [7M]  
(i)  $\overline{AB} + AC + \overline{BC} + \overline{BC} + AB$   
(ii)  $(A + B)(\overline{A} + C)(B + C)(\overline{A} + D)(B + D)$   
b) Reduce the following expression to the simplest possible POS and SOP forms. [7M]  
 $F = \sum m(6, 8, 13, 18, 19, 25, 27, 29, 31) + d(2, 3, 11, 15, 17, 24, 28)$

**UNIT-III**

- 5 a) What is a decoder? Draw the logic diagram of a 2 to 4 line decoder using NAND gates including an enable input. [7M]  
b) Give circuit implementation of 4 Bit Ripple adder and Ripple Adder/Subtractor using ones and twos complement method. [7M]

**(OR)**

- 6 a) Design a combinational circuit using ROM. The circuit accepts a 3 bit number and generates an output binary number equal to square of input number. [7M]  
b) Design and draw the logic circuit diagram for full adder/subtractor. Let us consider a control variable w and the designed circuit that functions as a full adder when  $w=0$ , as a full subtractor when  $w=1$ . [7M]



**UNIT-IV**

7 a) Draw the schematic circuit of an edge-triggered JK flip flop with active low preset and active low clear using NAND gates and explain its operation? [7M]

b) Analyze latch with NOR gates. Derive transition and state tables. [7M]

**(OR)**

8 a) Convert a JK flip flop into: [7M]  
i) SR flip flop ii) T flip flop iii) D flip flop

b) What is the drawback of JK flip flop? Design a flip flop which overcomes this drawback and explain with neat diagram. [7M]

**UNIT-V**

9 a) Implement a synchronous counter having the counting sequence as 2, 0, 3, 1, 2, 0, 3, 1.....using T-flip flop. [7M]

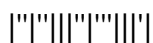
b) Draw and explain the operation of parallel-in parallel-out shift register. [7M]

**(OR)**

10 a) Explain the operation of 4-bit Johnson counter with circuit diagram, state transition diagram and state table. Draw the corresponding timing diagrams? [7M]

b) Design a 4-bit universal shift register using D flip flops and multiplexers? [7M]

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**UNIT-I**

- 1 a) What is the use of complements? Perform subtraction using 7's complement for the given Base-7 numbers (565)-(666). [7M]  
b) Explain various number systems and codes and their conversion with examples for each. [7M]

**(OR)**

- 2 a) Convert the following [7M]  
i)  $(53.625)_{10}$  to  $(?)_2$       ii)  $(3FD)_{16}$  to  $(?)_2$       iii)  $(A69.8)_{16}$  to  $(?)_{10}$   
b) Perform the subtraction in binary using 1's and 2's complement methods. [7M]  
(i)  $(97)_{10} - (255)_{10}$     ii)  $(1111101)_2 - (100111110)_2$     iii)  $(255)_{10} - (408)_{10}$

**UNIT-II**

- 3 a) State and prove the following laws of Boolean algebra. [7M]  
i) Commutative    ii) associative    iii) distributive    iv) idempotence    v) absorption  
b) Represent and draw the following Boolean function using minimum number of basic gates. i)  $(AB + AB')$     ii)  $[(ABD(C + D + E)) + (A + DBC)'] (ABC + (CAD)')$  [7M]

**(OR)**

- 4 a) Simplify the following Boolean expression. [7M]  
 $T(x, y, z) = (x + y) \{ [x' (y' + z')]'\} + x' y' + x' z'$   
 $X(A, B, C, D) = A^1 B^1 C^1 + (A+B+C^1)^1 + A^1 B^1 C^1 D$   
b) Reduce the following expression using k-map  $f = \prod M(1, 4, 5, 11, 12, 14) \cdot d(6, 7, 15)$ . [7M]

**UNIT-III**

- 5 a) What is a multiplexer? Design a 4\*1 multiplexer. Write the truth table and draw the logic diagram. [7M]  
b) Design a PAL for the following logical functions. [7M]  
 $Y_1 = AB + A'CB'$ ,  $Y_2 = AB'C + AB + AC'$ ,  $Y_3 = AB + BC + CA$

**(OR)**

- 6 a) Design a function  $F = ABC + (A+B+C)'$  by using 3 to 8 decoder. [7M]  
b) What is a PLD? Tabulate the comparisons between PLA, PAL and PROM. [7M]

**UNIT-IV**

- 7 a) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation. [7M]  
b) Distinguish between combinational and sequential circuits. List some applications of sequential circuits. [7M]

**(OR)**

- 8 a) Draw the circuit diagram of a positive edge triggered JK flip flop and explain its operation with the help of a truth table. [7M]  
b) Convert a D flip flop into SR flip flop and JK flip flop. [7M]

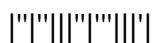
**UNIT-V**

- 9 a) Design a modulus 6 synchronous counter using JK flip-flop and also draw the timing diagrams. [7M]  
b) List the basic types of shift registers in terms of data movement with diagrams. [7M]

**(OR)**

- 10 a) Draw the state diagram of modulo-4 up/down counter. Explain its operation with the help of timing diagrams. [7M]  
b) Explain the design of ring counter using shift registers. [7M]

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**UNIT-I**

- 1 a) How are negative numbers represented? Represent signed numbers from +7 to -8 [7M]  
 using different ways of representation.
- b) Convert the following numbers into Gray code numbers [7M]  
 i)  $96_{10}$  ii)  $45_{16}$  iii)  $235_8$  iv)  $85_{12}$

**(OR)**

- 2 a) Subtract the following decimal numbers by the 9's and 10's complement methods. [7M]  
 $274 - 86$  ii)  $93 - 615$  iii)  $574.6 - 297.7$  iv)  $376.3 - 765.6$
- b) Express the Decimal Digits 0 - 9 in BCD, 84-2-1 and Excess-3. [7M]

**UNIT-II**

- 3 a) Simplify the following using K- map and implement the same using NAND gates. [7M]  
 $Y(A, B, C) = \sum (0, 2, 4, 5, 6, 7)$
- b) Derive and Implement Exclusive OR function involving three variables using only [7M]  
 NAND function.

**(OR)**

- 4 a) Simplify the following using K- map and implement the same using NOR gate. [7M]  
 $Y(A, B, C, D) = \sum (0, 2, 5, 7, 8, 10, 13, 15)$
- b) Obtain the simplified expression in product of sums. [7M]  
 i)  $F(A, B, C, D) = \pi(0, 1, 2, 3, 4, 10, 11)$  ii)  $F(A, B, C, D) = \pi(1, 3, 5, 7, 13, 15)$

**UNIT-III**

- 5 a) Explain the design procedure for multiplexers and draw the logic diagram of a 4- [7M]  
 to-1 line multiplexer with logic gates.
- b) Design an 8:3 encoder circuit? Write a HDL code for an 8:3 encoder and explain [7M]  
 the same briefly.

**(OR)**

- 6 a) What is a comparator? Explain the operation of a 2-bit comparator with a relevant [7M]  
 diagram. Draw its logic symbol and write a HDL code.
- b) Explain the working of n-bit subtractor with the help of neat block diagram? [7M]

**UNIT-IV**

- 7 a) Design a JK flip flop using AND gates and NOR gates. Explain the operation of [7M]  
 the JK flip flop with the help of characteristic table and characteristic equation.  
 Explain the Race around condition and also explain how to eliminate it.
- b) Draw the circuit diagram of clocked D-flip-flop with NAND gates and explain its [7M]  
 operation using truth table. Give its timing diagram.

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**R20**

**SET - 3**

**(OR)**

- 8 a) Draw the schematic circuit of a T flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation? [7M]  
b) Implement RS-latch using NAND and NOR gates? Explain its operation. [7M]

**UNIT-V**

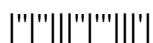
- 9 a) What is the primary disadvantage of an asynchronous counter? Explain the working of 4-bit asynchronous counter? [7M]  
b) Explain the operation of 4-bit serial in parallel out shift register with the help of neat diagrams. [7M]

**(OR)**

- 10 a) Design a 4-bit ring counter using D flip-flop. Draw and explain the circuit diagram and timing diagrams. [7M]  
b) List the basic types of shift registers and state various applications of shift register. [7M]

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**UNIT-I**

- 1 a) Perform the subtraction using 1's complement and 2's complement methods. [7M]  
 i) 11010 – 10000      ii) 11010 – 1101      iii) 100 – 110000  
 b) Find the 12-bit 1's complement form of the following decimal numbers. [7M]  
 i) -97    ii) -224    iii) -205.75    iv) -29.375

**(OR)**

- 2 a) Convert the following octal numbers to hexadecimal [7M]  
 i) 256    ii) 2035    iii) 1762.46    iv) 6054.263  
 b) What is a Gray code? Obtain a 3-bit and 4-bit gray code from a 2-bit gray code by reflection. [7M]

**UNIT-II**

- 3 a) Draw the logic symbol and construct the truth table for each of the following gates. [7M]  
 i) Two input NAND gate      ii) Three input NOR gate  
 iii) Two input Ex-OR gate      iv) Three input Ex-NOR gate  
 b) Convert the given expressions in standard SOP form [7M]  
 i)  $f(A,B,C)=A + AB + CB$     ii)  $f(P,Q,R)=PQ + R + PR$

**(OR)**

- 4 a) Using K-map method, simplify the POS expression for the Boolean function, [7M]  
 $Y(A,B,C,D) = \pi M(0,1,2,3,4,6,10,11)$  Implement the same using universal gates.  
 b) Convert the given expressions in standard POS form [7M]  
 i)  $f(A, B, C) = (A + B)(B + C)$     ii)  $f(P, Q, R) = (P + Q')(P + R)$

**UNIT-III**

- 5 a) Implement the following multiple output functions using PROM [7M]  
 $F1 = \sum m(0, 1, 4, 7, 12, 14, 15)$        $F3 = \sum m(2, 3, 7, 8, 10)$   
 $F2 = \sum m(1, 3, 6, 9, 12)$        $F4 = \sum m(1, 3, 5)$   
 b) Design a 32:1 multiplexer using two 16:1 and 2:1 multiplexers. [7M]

**(OR)**

- 6 a) What is programmable logic array? Draw and explain the block diagram of PLA? [7M]  
 b) Explain the design procedure for multiplexers and de-multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates. [7M]

**UNIT-IV**

- 7 a) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table. [7M]  
 b) Give the transition table for SR, JK, D and T flip flops. Convert an SR flip flop into D flip flop. [7M]

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**R20**

**SET - 4**

**(OR)**

- 8 a) What do you mean by sequential circuit? Explain with the help of block diagram? [7M]  
Give the comparisons between combinational and sequential circuits.
- b) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation? [7M]

**UNIT-V**

- 9 a) With the help of neat diagram explain the operation of 4-bit serial-in serial-out shift register? [7M]
- b) Draw the logic diagram of a 4-bit binary ripple counter using flip flops that trigger on negative edge transition? Explain the operation. [7M]

**(OR)**

- 10 a) How synchronous counters differ from asynchronous counter. Draw the complete timing diagram for the five-stage synchronous binary counter. [7M]
- b) What is shift register? Explain the different modes of operation of shift register? [7M]

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