Code No: R201221 **R20** SET - 1

I B. Tech II Semester Supplementary Examinations, March- 2022

DIGITAL LOGIC DESIGN

(CSE-CS&T, CSE-AI&ML, CSE-AI, CSE-DS, CSE-AI&DS, CSE-CS, CSE-IOT&CS INCL BCT, CSE-CS&BS,CSE-IOT, AI&DS, Cyber Security)

Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

UNIT-I

1 a) Express the following numbers in decimal: (7M)
   (i) $(26.24)_8$
   (ii) $(DADA.A)_{16}$

   b) Represent the decimal number 1,999 in: (i) BCD, (ii) 84-2-1 code, (iii) 2421 code. (7M)

Or

2 a) Express the following numbers in binary: (7M)
   (i) $(27.315)_{10}$
   (ii) $(16.5)_{16}$

   b) Perform the subtraction on the given unsigned binary numbers using the 1's and 2's complement methods: 100010-100110. (7M)

UNIT-II

3 a) Draw the logic diagram corresponding to the following Boolean expressions without simplifying them: (7M)
   (i) BC′+AB+ACD
   (ii) (AB+A′B′)(CD′+C′D)

   b) Simplify the Boolean function using K-map in sum of products form: (7M)
   F(w,x,y,z)=∏(0,1,2,3,4,10,11).

Or

4 a) Simplify the following expression and implement with two-level NOR gate circuits: (7M)
   AB′C+B′C′D′+BCD+ACD′+A′B′C+A′BC′D

   b) Simplify the Boolean function using K-map in sum of products form and draw the logic diagram after simplification: (7M)
   F(A,B,C,D)=Σ(0,2,4,5,6,7,8,10,13,15).

UNIT-III

5 a) Design a 2-bit comparator with basic gates. (7M)

   b) Write and verify a gate-level hierarchical HDL model of the 4-to-16-line decoder circuit. (7M)

Or

6 a) Design a 3-to-8 decoder with only 2-input NAND gates. (7M)

   b) A combinational circuit is defined by the functions: (7M)
   $F_1(A,B,C)=\Sigma(3,5,6,7)$; $F_2(A,B,C)=\Sigma(0,2,4,7)$.
   Implement the circuit with PLA.

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UNIT-IV

7	a)	Explain the principle of T Flip-flop with the help of logic diagram and excitation table.	(7M)
	b)	Convert the JK Flip-flop into D Flip-flop.	(7M)

Or

8	a)	Explain the principle of JK Flip-flop with the help of logic diagram and truth table.	(7M)
	b)	Convert the T Flip-flop into D Flip-flop.	(7M)

UNIT-V

9	a)	Design a mod-12 counter using T flip-flops.	(7M)
	b)	Explain the operation of 4-bit left shift register with JK flip-flops.	(7M)

Or

10	a)	Explain the operation of a 4-bit shift register with parallel load using D flip-flops.	(7M)
	b)	Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use D flip-flops. Treat the un-used states as don't-care conditions.	(7M)