

II B. Tech I Semester Supplementary Examinations, July - 2023
ELECTRONIC DEVICES AND CIRCUITS
 (Electrical and Electronics Engineering)

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions, each Question from each unit
 All Questions carry **Equal** Marks

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 UNIT-I

- 1 a) Explain energy band diagram of insulator, semiconductor and conductor. [8M]  
 b) The current flow through a PN-junction germanium diode is 40 mA for a forward biased voltage of 0.5V at 300K. Calculate the static and dynamic resistances of the diode. [6M]

Or

- 2 a) Explain about drift and diffusion currents in semiconductors. [8M]  
 b) The current flow through a PN-junction diode is 0.65 mA at forward-biased voltage 350 mV and 20 mA at forward-biased voltage 450 mV. Determine the value of  $\eta$  if the junction operates at 295K. [6M]

UNIT-II

- 3 a) With a neat sketch explain the construction and working of SCR. [8M]  
 b) Draw and explain the V-I characteristics of the UJT. [6M]

Or

- 4 a) With neat sketch explain the operation of full wave rectifier with capacitor filter and derive the expression for ripple factor. [10M]  
 b) Give the comparison of various filter circuits in terms of ripple factors. [4M]

UNIT-III

- 5 a) Define  $\alpha$ ,  $\beta$  and  $\gamma$  of a transistor. Show how they are related to each other. [7M]  
 b) Explain the various current components in a transistor. [7M]

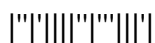
Or

- 6 a) Explain the principle of operation of enhancement MOSFET. [7M]  
 b) A self-biased p-channel JFET has a pinch-off voltage of  $V_p=5V$  and  $I_{DSS}=12mA$ . The supply voltage is 12V. Determine the values of  $R_D$  and  $R_S$  so that  $I_D=5mA$  and  $V_{DS}=6V$ . [7M]

UNIT-IV

- 7 a) Explain about DC Load line and the significance of Q-point. [5M]  
 b) Design a self-bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications:  $V_{CC}=16V$ ,  $V_{BE}=0.7V$ ,  $V_{CEQ}=8V$ ,  $I_{CQ}=4 mA$  and  $\beta=50$ . [9M]

Or



- 8 a) Derive an expression for the condition to avoid thermal runaway. [7M]  
b) Design a voltage divider bias circuit for specified condition  $V_{CC} = 12V$ ,  $V_{CE} = 6V$ ,  $I_C = 1 \text{ mA}$ ,  $S = 20$ ,  $\beta = 100$  and  $V_E = 1V$ . [7M]  
UNIT-V
- 9 a) Explain the principle of operation of CS amplifier with the help of circuit diagram. [6M]  
b) Determine the current gain, input impedance and voltage gain when the transistor is connected in CB configuration with a load  $R_L = 10K\Omega$ ,  $V_{CB} = 10V$ ,  $I_C = 1 \text{ mA}$ ,  $h_{ib} = 20\Omega$ ,  $h_{rb} = 5 \times 10^{-4}$ ,  $h_{fb} = -0.98$ ,  $h_{ob} = 10^{-7} \text{ } \Omega$ . [8M]
- Or
- 10 a) Derive the expressions for input impedance, output impedance and voltage gain of JFET Common Drain amplifier. [9M]  
b) Define the various h-parameters and give their units. [5M]

