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II B. Tech I Semester Supplementary Examinations, July - 2023 ELECTRONIC DEVICES AND CIRCUITS			
(Com to ECE, EIE, ECI) Time: 3 hours Max. Mar			arks: 70
Answer any FIVE Questions, each Question from each unit All Questions carry Equal Marks			
UNIT-I			
1	a)	What are the majority and minority carriers in an trivalent impurity semiconductors? Explain in detail.	[7M]
	b)	Derive the expression for Fermi level in p-type semiconductors.	[7M]
2	a)	Or Draw the energy band diagram for (i) Conductors (ii) Insulators (iii) Semiconductors Explain in detail	[7M]
	b)	Discuss about Diode Resistance & Diode capacitance. UNIT-II	[7M]
3	a)	With neat diagrams, explain the construction of SCR and give its characteristics.	[7M]
	b)	Explain the construction and working of full wave rectifier.	[7M]
		Or	
4	a)	Explain Break down mechanisms in a Zener diode?	[7M]
	b)	A 50Ω load resistance is connected across a half wave rectifier. The input supply voltage is 230V (rms) at 50 Hz. Determine the DC output (average) voltage, peak-to-peak ripple in the output voltage (Vp-p), and output ripple frequency (fr).	[7M]
5	a)	UNIT-III Explain the operation of BIT. Give the relationship between α , β and γ of a	[7M]
5	a) b)	transistor. Find the ripple factor expression for FWR with inductor filter.	[7M]
	,	Or	
6	a)	Explain input and output characteristics of CE configuration.	[7M]
	b)	Explain the operation of JFET. Write some applications for JFET. UNIT-IV	[7M]
7	a)	Explain the Voltage Divider Biasing With neat sketch.	[7M]
	b)	Explain the procedure to draw AC and DC load lines.	[7M]
		Or	
8	a)	What is meant by bias stability? How you stabilize the operating point?	[7M]
	b)	Write a short notes on different biasing techniques for FET. UNIT-V	[7M]
9		Draw the circuit of source follower Amplifier and derive the expressions for A1, Av, R_i and R_0 .	[14M]
10		Or	
10	a)	Explain the hybrid small signal model for common collector configuration.	[/M]
	b)	What is the significance of two post networks? Explain	[7M]
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