Code No: R2021042 **R20** SET - 1

II B. Tech I Semester Regular/Supplementary Examinations, December-2023
SWITCHINNG THEORY AND LOGIC DESIGN
(Com to ECE, EIE, ECT)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1 a) Convert the number $(127.75)_8$ to base 10, base 3, base 16 and base 2. [7M]

b) Perform subtraction on the following unsigned binary numbers using the 2's complement of the subtrahend (a) $(11011)_2$-$(11001)_2$ (b) $(110100)_2$-$(10101)_2$ [7M]

OR

2 a) Given the 4 bit data word 1011, generate the hamming code that corrects and detects single errors and also explain the error correction capability. [7M]

b) Express the function Y = A + B'C in canonical SOP and canonical POS form. [7M]

UNIT-II

3 a) Simplify the following function using K-map. F(A,B,C,D) = Σ(1,3,4,5,6,11,13,14,15) [7M]

b) Assess a full adder using two half adders and an OR gate. [7M]

OR

4 a) Design a code converter for BCD to gray code conversion [7M]

b) For the given function T(w,x,y,z) = Σ (0,1,5,7,8,10,14,15) [7M]
i) Show on the map ii) Find all prime implicants and indicate which are essential. iii) Find a minimal expression

UNIT-III

5 a) Design a priority encoder using logic gates. [7M]

b) Implement the following functions using PLA with three inputs, four product terms and two outputs. F1 (A, B, C) = ∑m (3, 5, 6, 7), F2 (A, B, C) = ∑m (0, 2, 4, 7). [7M]

OR

6 a) Implement F=Σ(0,1,2,3) using decoder, [7M]

b) Draw the pin diagrams of Ics 7442 and 7447. Explain their functions. [7M]

UNIT-IV

7 a) Draw the state diagram and characteristic table of Master Slave JK flip-flop. [7M]

b) Design a 3 bit synchronous up counter using T Flip-flops [7M]

OR

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8 a) Design a 4-bit ring counter and mention its applications. [7M]

b) Convert SR flip – flop to T flip – flop. [7M]

UNIT-V

9 a) Identify a Mealy model of sequence detector to detect the pattern 1001. [7M]

b) Define equivalent state. Write the benefits of state reduction. [7M]

OR

10 a) Reduce the number of states in the following state table and tabulate the reduced state table shown below: [7M]

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

b) Differentiate between Mealy and Moore machine with examples. [7M]

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UNIT-I

1	a)	Perform the following conversions i) FD3.6A to Octal ii) $(673.62)_8$ to decimal iii) (793.75)10 to Hexa decimal	[9M]
	b)	Rewrite the expression A+BC in standard product of sum form.	[5M]

OR

2	a)	What you mean by weighted code? Explain with suitable examples.	[7M]
	b)	Simplify the following function and realize using universal gates F(A,B,C) = A'BC' + ABC + B'C' + A'B'	[7M]

UNIT-II

3	a)	Simplify the following using Tabular method. F(A,B,C,D) = Σ(3,7,8,12,13,15)+ dΣ(9,14)	[7M]
	b)	List the advantages and disadvantages of minimization of Boolean Function using K-Map.	[7M]

OR

4	a)	Explain how a look ahead adder speeds up the addition process. Draw the architecture.	[7M]
	b)	Discuss in detail, the working of full adder logic circuit.	[7M]

UNIT-III

5	a)	Design a full adder using Multiplexer.	[7M]
	b)	Draw and explain the logic diagram of a 2-to-4 decoder using NOR gates only. Include an enable input.	[7M]

OR

6	a)	Implement f (A,B,C,D) = ∑(0,1,3,5,6,8,9,11,12,13) using PAL and explain its procedure .	[7M]
	b)	Explain the working of a De-multiplexer with the help of an example.	[7M]

UNIT-IV

7	a)	Explain the operation, state diagram and characteristics of a T-Flip flop.	[7M]
	b)	Write the differences between synchronous and asynchronous counters.	[7M]

OR

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8 a) Design and explain the working of a synchronous MOD-5 counter. [7M]

b) Explain the term Race around condition. How is it satisfied by Master-slave Flip-Flops. [7M]

UNIT-V

9 a) Convert the following Mealy machine into a corresponding Moore machine: [10M]

Present State	Next State			
	a		b	
	State	O/P	State	O/P
q_1	q_1	1	q_2	0
q_2	q_4	1	q_4	1
q_3	q_2	1	q_3	1
q_4	q_3	0	q_1	1

b) What is FSM state? List its two basic types. [4M]

OR

10 a) What is meant by state diagram? Define how state assignment is important in a sequential circuit design. Describe with a suitable example. [7M]

b) Design a FSM which detects 0011 pattern and set z = 1 for all other patterns z = 0 [7M]

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UNIT-I

1 a) Assess the following Excess-3 numbers into decimal numbers. [7M]
(i) $(1011)_2$ (ii) $(1001\ 0011\ 0111)_2$
b) Simplify the following: i) (A+ AC + B) ii) F = AB(C +C) + AB [7M]
iii) F = (X +Y)(X + Z)

OR

2 a) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Examine the method of detecting the error using Hamming code. [7M]
b) What are the universal gates? Why they are called universal gate? [7M]

UNIT-II

3 a) Simplify the Boolean function using K map technique: [7M]
F = π M (3, 4, 6, 7, 11, 12, 13, 14, 15).
b) Explain a binary adder, which can be used to add two binary numbers? [7M]

OR

4 a) Design a Half Subtractor. [7M]
b) By using tabulation methods simplify the function: [7M]
$Z = f(A,B,C) = A'B'C' + A'B'C + AB'C' + AB'C$

UNIT-III

5 a) Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux. [7M]
b) What is PAL? How does it differ from PROM and PLA? [7M]

OR

6 a) Draw the logic circuit of a 3 to 8 decoder and explain its working. [7M]
b) Draw the logic diagram of 1 to 4 line demultiplexer and discuss on it. [7M]

UNIT-IV

7 a) Design a BCD counter using JK Flip-Flops. [7M]
b) Analyze SISO and PIPO shift registers with neat logic diagram. [7M]

OR

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8 a) Implement D and T FFs using JK flip flop. Tabulate the characteristics equation of the three flip flops. [7M]

b) Draw the pin diagrams of Ics 7490 and 74121. Explain their functions. [7M]

UNIT-V

9 a) A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations: A (t+1) = AX+BX; B (t+1) = A'X; Y= (A+B) X'. [8M]

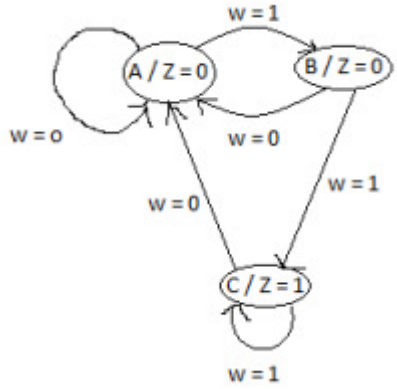
(i) Construct the state table.

(ii) Draw the state diagram.

b) Write the usage of Mealy machine with example. [6M]

OR

10 a) For the given state diagram, prepare the state table , state assignment and state reduction tables. [9M]



b) Examine the state assignment problem. Define its rule. [5M]

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UNIT-I

1 a) Describe the procedure to get the Hamming code for the binary word 1101100. [7M]
b) State and Prove the postulates of Boolean Algebra. [7M]

OR

2 a) Deduce $FACE_{16}$ in its binary, octal and decimal equivalent. [7M]
b) Interpret OR gate and AND gate using NAND gates. [7M]

UNIT-II

3 a) Simplify the following function using Karnaugh Map. [7M]
$F(W,X,Y,Z)=\sum m(0,1,3,9,10,12,13,14)+\sum d(2,5,6,11)$.
b) Construct BCD adder and explain the operation. [7M]

OR

4 a) Design a 4 bit BCD to Excess-3 code converter [7M]
b) Use the K-map method to simplify the following 5-variable function [7M]
$F = \sum(3,6,7,8,10,12,14,17,19,20,21,24,25,27,31)$

UNIT-III

5 a) Design a 64:1 MUX using 8:1 MUXs. [7M]
b) Draw the pin diagrams of IC 7485 and IC 74154. Explain their functions. [7M]

OR

6 a) Design a 4 bit comparator circuit using logic gates. [7M]
b) Implement the following Boolean function using PLA [7M]
$F_1(w.x.y.z) = \sum(0,1,3,5,9,13)$
$F_2(w,x,y,z) = \sum(0,2,4,5,7,9,11,15)$

UNIT-IV

7 a) Analyze the circuit of a SR flip flop and realize SR flip flop using D flip flop. [7M]
b) Draw the pin diagrams of IC 7474 and IC 7475. Explain their functions. [7M]

OR

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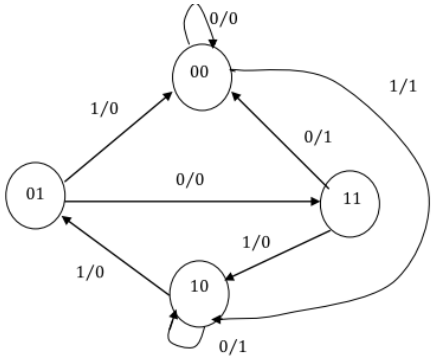
8 a) Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load. [7M]

b) Draw a block diagram of Modulo 10 ripple counter and explain its timing diagram. [7M]

UNIT-V

9 a) Show the state transition diagram of a sequence detector circuit that detects '1010' from input data stream using Moore model. [7M]

b) A sequential circuit has one input and one output. The state diagram is shown below: [7M]



Design the sequential circuit with D flip-flop

OR

10 a) Convert the following Moore machine into a corresponding Mealy machine: [7M]

Present State	Next State		Output
	w=o	*w=1*	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	E	0

b) Write the usage of Moore machine with example. [7M]

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