Code No: R2021042 **R20** SET - 1

II B. Tech I Semester Regular/Supplementary Examinations, January-2023
SWITCHINNG THEORY AND LOGIC DESIGN
(Com to ECE, EIE, ECT)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1	a)	Given the 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors.	[7M]
	b)	Explain the logic gates with it symbol and truth table.	[7M]

OR

2	a)	The binary numbers listed have a sign bit in the left most position and, if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. (i) 101011 + 111000 (ii) 001110 + 110010 (iii) 111001 – 001010 (iv) 101011 – 100110	[7M]
	b)	Convert the following to Decimal and then to octal (i) (125F)16 (ii) (10111111)2(iii) (4234)10	[7M]

UNIT-II

3	a)	Find the complement and duality of given function below and then reduce minimum number of literals in each case F =$\left[\left(\overline{ab}\right).a\right]\left[\left(\overline{ab}\right).b\right]$	[7M]
	b)	Simplify the following to minimum number of literals (i)$\bar{A}$B($\bar{D}+\bar{C}$D)+B(A+$\bar{A}CD$) (ii)$\bar{x}\bar{y}$+xy+$\bar{x}y$	[7M]

OR

4	a)	Design a full adder by using two half adders	[7M]
	b)	With neat block diagram, explain BCD adder circuit.	[7M]

UNIT-III

5	a)	Design and implement Full adder with PLA.	[7M]
	b)	Write the comparisons between PAL, PLA.	[7M]

OR

6	a)	Design an 8 to 3 priority encoder.	[7M]
	b)	Draw the pin diagram and explain the functions of ICs 7442 and 7447.	[7M]
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UNIT-IV

7 a) What is a flip-flop? Design the basic flip-flop using NOR gates and explain. [7M]

b) What is an excitation table? Write the excitation tables for JK and T flip-flops. [7M]

OR

8 a) Write the differences between synchronous and Asynchronous Counters. [7M]

b) Explain the operation of 4-bit asynchronous counter. [7M]

UNIT-V

9 a) Draw the diagram of Mealy type FSM for serial adder. [7M]

b) Draw the circuit for Moore type FSM. [7M]

OR

10 a) Write the difference between mealy and moore machines. [7M]

b) Convert the given mealy machine to moore machine by using transition diagram [7M]

State	Input		Out put
	a	b	
A	B	A	0
B	B	C	0
C	B	D	0
D	B	A	1

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UNIT-I

1	a)	Convert the given expression in standard SOP form f (A,B,C) = AC+BA+BC.	[7M]
	b)	Convert the given expression in standard POS form y=A.(A+B+C).	[7M]

OR

2	a)	Subtract the following numbers in 9's complement form (i)72532-03250 (ii) 03250 -72532	[7M]
	b)	Explain how 1's complement and 2's complement of a binary number is obtained? Illustrate by an example.	[7M]

UNIT-II

3	a)	Reducing the following function using K- map F(A,B,C,D) =∑m(5,6,7,8,9,12,13,14)	[7M]
	b)	Implement the following Boolean function using AND ,OR and inverter gates $\overline{(AB + CD + E)}$	[7M]

OR

4	a)	Design a combinational circuit that access a 3 bit number and generates output number which is equal to square of the input.	[7M]
	b)	Design an excess-3 adder using 4-bit parallel binary adder and logic gates.	[7M]

UNIT-III

5	a)	Implement the following Boolean functions using PLA. A(x,y,z)=∑(1,2,4,6), B(x,y,z)= ∑(0,1,6,7), and C(x,y,z)= ∑(2,6).	[7M]
	b)	Design a combinational circuit using PROM that accepts 3-bit binary number and generates its equivalent excess -3 code.	[7M]

OR

6	a)	Design a 16×1 MUX by using two 8×1 MUX.	[7M]
	b)	Draw the pin diagrams and their functions of ICs 7485 and 74154.	[7M]

UNIT-IV

7	a)	Draw the diagram of master slave JK flip-flop.	[7M]
	b)	Convert the JK flip-flop into a T flip-flop.	[7M]

OR
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8	a)	Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table.	
	b)	Discuss the Johnson counter with neat diagram.	[7M]

UNIT-V

9	a)	Draw the circuit for Moore type FSM.	[7M]
	b)	Draw the state diagram of mod-8 Up - Down counter in Moore model and obtain its state table.	[7M]

OR

10	a)	What is meant by sates reduction? Explain what are the advantages of state reduction in sequential circuits?	[7M]
	b)	Draw a state diagram of a sequence detector which can detect 101.	[7M]

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Answer any **FIVE** Questions, each Question from each unit
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UNIT-I

1	a)	Implement a 3 - level logic circuit using NOR gates for $F= (AB^{'}+CD^{'})(A^{'}+B)$	[7M]
	b)	Represent and draw the following Boolean function using minimum number of Basic gates. i) (AB + AB’) (AB)’ ii) [(ABD(C + D + E)) + (A +DBC)’] (ABC + (CAD)’)	[7M]

OR

2	a)	Represent the decimal numbers 0 to 7 ,-7 to -1 in signed magnitude, 1’s complement, 2’s complement forms using 4-bits.	[7M]
	b)	Explain about weighted and Non weighted codes.	[7M]

UNIT-II

3	a)	Reduce the following function using K- map $F = \pi M(3,4,5,6,7,12,13)+d(8,10,14,15)$	[7M]
	b)	Draw logic diagram of Ex-OR and EXNOR gate using NAND gate and prove it using Boolean equation and truth table.	[7M]

OR

4	a)	Write the differences between sequential and combinational circuits with an example.	[7M]
	b)	Design a 4-Bit Adder subtractor circuit by using a full adder.	[7M]

UNIT-III

5	a)	Design a 1 to 8 Demultiplexer with diagram and truth table.	[7M]
	b)	Design a 4-bit digital comparator.	[7M]

OR

6	a)	Design a BCD to excess -3 code converter and implement using suitable PLA.	[7M]
	b)	Implement the following functions using a PROM i) $F(w,x,y,z)=\sum(1,9,12,15)$ ii) $G(w,x,y,z)= \sum(0,1,2,3,4,5,7,8,10,11,12,13,14,15)$	[7M]
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UNIT-IV

7 a) Explain about the operation of Clocked RS flip flop. [7M]

b) Design a D type positive edge triggered flip-flop. Explain the operation of the sequential circuit when clock pulse equal to 1. [7M]

OR

8 a) Draw the logic diagram of a JK flip - flop and using excitation table explain its operation. [7M]

b) Draw and explain the operation of 4 bit ring counter. [7M]

UNIT-V

9 a) Discuss about the procedure of Mealy to Moore conversion. [7M]

b) Explain about sequential circuits, state table and state diagram. [7M]

OR

10 a) Write the differences between synchronous and asynchronous counters [7M]

b) Convert the following Moore machine to mealy machine by using transition diagram [7M]

State	Input		Out put
	0	1	
A	B	A	b
B	B	C	b
C	B	A	a

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Answer any **FIVE** Questions, each Question from each unit
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UNIT-I

1 a) How do you convert a gray number to binary? Generate a 4-bit gray code directlyusing the mirror image property. [7M]

b) Write the comparisons between 1's complement and 2's complement . [7M]

OR

2 a) What are the differences between canonical form and standard form? Explain [7M]

b) Convert the following expression into SOP and POS [7M]
(i) (AB+C)(B+$\bar{C}D$) (ii)$\bar{x}$+(x+$\bar{y}$)(y+$\bar{z}$)

UNIT-II

3 a) Simplify the following [7M]
(i)AB+ BC+ A^{l}C = AB+ A^{l}C (ii) (X+Y).(Y^{l}+Z) = X

b) Simplify the following using K- map and implement the same using NAND gates. Y (A, B, C) =∑(0,2,4,5,6,7) [7M]

OR

4 a) Design a Binary to BCD code converters using K-map. [7M]

b) Convert the BCD to XS-3 and XS-3 to BCD by using a full adder [7M]

UNIT-III

5 a) Design and implement Full adder with PLA. [7M]

b) Design a combinational circuit using PROM. The circuit accepts a 3 bit number and generates an O/p binary number equal to square of input number. [7M]

OR

6 a) Realize the following four Boolean functions using PAL. [7M]
F1(w,x,y)=∑m(1,2,4,6)
F2(w,x,y)= ∑m(0,1,6,7)
F3(w,x,y)= ∑m(2,6)

b) Implement the following functions using a PROM: i) F(w,x,y,z)=∑(1,9,12,15) ii) G(w,x,y,z)==∑(0,1,2,3,4,5,6,7,10,11,12,13,14,15) [7M]
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UNIT-IV

7 a) What is Race condition and explain about the operation of clocked RS flip-flop [7M]

b) Convert the JK Flip flop into RS flip-flop. [7M]

OR

8 a) What is a counter? implement and explain the basic operation of 4-bit up counter [7M]

b) With neat diagram explain the operation of 3-bit universal shift register. [7M]

UNIT-V

9 a) A clocked sequential circuit is provided with a single input x and single output z, Whenever the input produces a string pulsed 111 or 000 and at the end of the sequence it produces an output z=1 and overlapping is also allowed. Obtain state diagram and state table. [7M]

b) Differentiate the mealy machine from Moore machine. [7M]

OR

10 Explain the following with an example for each. [14M]
(i) State table (ii) State diagram (iii) State reduction.