Code No: R2022061 **R20** **SET - 1**

II B. Tech II Semester Supplementary Examinations, December - 2022

COMPUTER ORGANIZATION& ARCHITECTURE

(Common to CST, CSE(CS), CSE(IOTCSIBCT), CSE(IOT) &CS)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks

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UNIT – I

1 a) What is the use of compliment operation in digital computers? Explain r's and (r-1)'s complement. [7M]

b) Multiply $(-7)_{10}$ with $(3)_{10}$ by using Booth's multiplication. Give the flow table of the multiplication. [7M]

Or

2 a) Perform the arithmetic operations (+42) + (- 13) and (-42) - (- 13) in binary using signed-2's complement representation for negative numbers. [7M]

b) Discuss hardware implementation for signed magnitude for addition and subtraction. [7M]

UNIT – II

3 a) Register A holds the 8-bit binary11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to
i) 01101101 ii) 11111101 [7M]

b) Discuss about Common Bus System of basic computer Registers and memory. [7M]

Or

4 a) What is register transfer language? Explain the basic symbols used in register transfer. [7M]

b) What is the difference between a direct and an indirect instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? [7M]

UNIT – III

5 a) Explain about micro programmed control organization with neat sketch. [7M]

b) What is a stack? What is the need for stack memory in computers? Discuss the organization of stack. [7M]

Or

6 a) Define the terms Microinstruction, Microprogram, Control word and Control memory. [6M]

b) An instruction is stored at location 300 with its address field at location 301. The address filed has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is
i) direct ii) immediate iii) relative iv) register indirect
v) index with R1 as the index register [8M]

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UNIT – IV

7 Discuss in detail about Cache memory mapping techniques with neat diagram. [14M]

Or

8 a) What is page replacement mechanism? Discuss about LRU algorithms with example. [7M]

b) Explain how Handshaking Asynchronous data transfer is advantageous over strobe control data transfer. [7M]

UNIT – V

9 a) Explain Flynn's Classification of Computer system with an example. [7M]

b) Discuss about the major difficulties that cause the instruction pipeline to deviate from its normal operation. [7M]

Or

10 a) Give the block Diagram of a Crossbar Switch connected to one Memory module. [7M]

b) How to handle the branch instructions in instruction pipelining? Explain. [7M]