Code No:R2022061 **R20** **SET - 1**

II B. Tech II Semester Regular Examinations, June/July - 2022
COMPUTER ORGANIZATION& ARCHITECTURE
(Common to CST, CSE(CS), CSE(IOTCSIBCT), CSE(IOT) &CS)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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UNIT – I

1 a) Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 215 in (i) binary (ii) binary-coded octal (iii) binary-coded hexadecimal (iv) binary-coded decimal (BCD) [7M]

b) Derive and explain an algorithm for adding and subtracting 2 floating point binary numbers. [7M]

Or

2 a) Perform the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is a sign reversal. [7M]

b) Discuss hardware implementation of the booth's multiplication. Discuss with an example. [7M]

UNIT – II

3 a) Design a Full - subtractor circuit with three inputs X, Y, Z and outputs D, B. The circuit subtracts X - Y - Z where Z is the input borrow, B is the output borrow and D is the difference. Draw the circuit using NAND gates. [7M]

b) Explain different memory reference instructions. [7M]

Or

4 a) Briefly explain the arithmetic logic shift unit. [8M]

b) What are registers? Explain the use of accumulator and program counter registers used in computers. [6M]

UNIT – III

5 What are the different fields in the instruction format? Evaluate R = (X*Y) +(A-B) arithmetic statement using 0 address, 1 address, 2 address and 3 address instruction formats. [14M]

Or

6 a) Explain the concept of address sequencing for control memory. [8M]

b) Write the major characteristics of RISC and explain. [6M]

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UNIT – IV

7 a) What is the difference between synchronous and asynchronous data transfer? [7M]

b) What is virtual memory? How is it realized? Explain its use. [7M]

Or

8 a) Explain about Input-output interface with an example. [7M]

b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words for main memory. The main memory size is 128K X 32 [7M]
i) Formulate all pertinent information required to construct the cache memory.
ii) What is the size of the cache memory?

UNIT – V

9 a) Write about the SIMD array processor organization. [7M]

b) Explain the vector processing with suitable applications. [7M]

Or

10 a) Write short notes on Shared Memory Multiprocessors. [7M]

b) Describe in detail about pipeline processing. [7M]