Code No: R2022421 **R20** **SET - 1**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

COMPUTER ORGANIZATION

(Common to CSE(AIML),CSE(AI),CSE(DS),CSE(AIDS),CSD, AIDS & AIML)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1 a) Describe the functions of the main hardware components of a general purpose computer. [7M]

b) Subtract $(136)_8$ from $(636)_8$ using 8's complement method. [7M]

Or

2 a) What is a Floating point number? Explain the standard floating point representation with an example. [7M]

b) With a neat flow chart, explain the division of two fixed point numbers with an example. [7M]

UNIT-II

3 a) Explain the internal organization of a Digital computer. [7M]

b) Explain the phases of instruction cycle with a neat flow chart. [7M]

Or

4 a) Give a brief account on general purpose registers in CPU. [7M]

b) List out and explain the memory reference instructions. [7M]

UNIT-III

5 a) What is the role of Stack data structure in computer architecture? Explain the PUSH and POP instructions. [7M]

b) What is an Instruction format? Explain about various basic computer instruction formats. [7M]

Or

6 a) Briefly discuss the three main types of Data Transfer and Manipulation instructions. [7M]

b) With neat diagram, explain the address selection for control memory. [7M]

UNIT-IV

7 a) Describe the characteristics and advantages of Cache memory. [7M]

b) Draw the block diagram of DMA controller and explain its key components. [7M]

Or

8 a) With a neat diagram, show the memory address map of RAM and ROM for a computer system (Assume 512 bytes). [7M]

b) Explain the hardware organization of associative memory with a neat block diagram. [7M]

UNIT-V

9 a) What is an NXN cross bar switch? Write about the Clos multistage interconnection network. [7M]

b) Explain about Arithmetic and Instruction pipelines. [7M]

Or

10 a) Illustrate on RISC pipeline in detail. Explain any two types of interconnection structures. [7M]

b) Explain the types of Array processors in detail. [7M]

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Code No: R2022421 **R20** **SET - 2**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

COMPUTER ORGANIZATION

(Common to CSE(AIML),CSE(AI),CSE(DS),CSE(AIDS),CSD, AIDS & AIML)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1 a) Explain about the different types of Buses in computer architecture. [7M]

b) Explain about various types of complement's for a Binary number with suitable examples. [7M]

Or

2 With a neat flow chart, explain the working of Booths multiplication algorithm and also illustrate the steps to Multiply the two numbers 23 and -9 by using the Booth's multiplication algorithm. [14M]

UNIT-II

3 a) List out and explain the basic Arithmetic Micro operations. [7M]

b) What is an Interrupt and its types? Explain the flowchart of Interrupt cycle. [7M]

Or

4 a) Describe the data transmission between CPU registers during the execution of instructions through Register transfer notation. [7M]

b) Write about Control functions and Micro operations of a basic computer. [7M]

UNIT-III

5 a) What are the typical elements of a machine instruction? Explain. [7M]

b) With a neat diagram, explain the design of control unit and also explain its inputs and outputs. [7M]

Or

6 What is the need for designing the micro-instruction sequencing technique? Briefly discuss various micro-instruction sequencing techniques. [14M]

UNIT-IV

7 a) Discuss various possible modes of Data transfer to and from the peripherals in a computer system. [7M]

b) Describe the characteristics of Cache memory. Explain Write-through and Write-back methods. [7M]

Or

8 Explain the following [14M]
i)Auxilliary memory ii)Associative memory

UNIT-V

9 a) Explain the phases of Instruction pipeline with a neat flow chart. [7M]

b) Discuss various hardware implementations of Inter-processor synchronization [7M]

Or

10 a) Describe the characteristics of Multi processors. [4M]

b) Differentiate between Time Shared Bus, Crossbar Switch & Multiport Memory inter connection structures. [10M]

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Code No: R2022421 **R20** **SET - 3**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

COMPUTER ORGANIZATION

(Common to CSE(AIML),CSE(AI),CSE(DS),CSE(AIDS),CSD, AIDS & AIML)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit

All Questions carry **Equal** Marks

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UNIT-I

1 a) How to find r's complement and (r-1)'s complement of a number? Illustrate the same for $(563)_8$. [7M]

b) With a neat flow chart, explain the subtraction of two floating point numbers. [7M]

Or

2 a) Write the differences between RAM and ROM. [7M]

b) Explain the sequence of steps to detect an error using Cyclic Redundancy Check with a suitable example. [7M]

UNIT-II

3 a) Mention all Logic micro operations and explain their hardware implementation. [10M]

b) Explain the implementation of Circular and Arithmetic shift operations. [4M]

Or

4 a) Draw the circuit for Arithmetic Logic Shift unit and Explain its operations by giving its function table. [12M]

b) What do you mean by Interrupt in Computer architecture? [2M]

UNIT-III

5 List and explain in detail various addressing modes of a computer with example. [14M]

Or

6 a) Draw the block diagram for RISC processor architecture and explain its instruction set. Also discuss its advantages and disadvantages. [10M]

b) Define the terms [4M]

i) Control Memory ii) Micro Instruciton

UNIT-IV

7 a) What is cache memory? Explain how it enhances speed of accessing data. [7M]

b) What is a Virtual Memory? Explain the process of converting virtual addresses to physical addresses with a neat diagram [7M]

Or

8 a) What is Asynchronous Data Transfer? Explain any one method to achieve the asynchronous way of data transfer. [7M]

b) Explain Priority interrupt and Daisy chain interrupt system with necessary diagrams. [7M]

UNIT-V

9 a) List out the benefits of Multiprocessing? Give the important characteristics of multiprocessor systems. [7M]

b) Explain the five stages of RISC pipeline. [7M]

Or

10 a) What is the basic component of a Multi-stage switching network? Explain the structure of 8X8 omega switching network. [7M]

b) How does Parallel processing work? Discuss the use cases of Parallel processing. [7M]

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Code No: R2022421 **R20** **SET - 4**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

COMPUTER ORGANIZATION

(Common to CSE(AIML),CSE(AI),CSE(DS),CSE(AIDS),CSD, AIDS & AIML)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1	a)	Explain in brief about Weighted and Non-Weighted codes with one example each.	[7M]
	b)	How to find r's complement and (r-1)'s complement of a number? Illustrate the same for $(7654)_8$.	[7M]

Or

2	a)	With an example, explain the CRC code for detecting multiple errors in a message.	[7M]
	b)	With a neat flow chart, explain the Floating point Multiplication algorithm with an example.	[7M]

UNIT-II

3	a)	Explain the hardware implementation of Shift Micro operations.	[7M]
	b)	Explain the implementation of Binary Adder and Binary Incrementor.	[7M]

Or

4	a)	Explain the Instruction cycle execution with Interrupts.	[7M]
	b)	Enumerate the concept of RTL in detail.	[7M]

UNIT-III

5	a)	Evaluate the arithmetic statement X=(A+B) * (C+D) using Three-address, Two-address, One-address and Zero-address instruction formats.	[7M]
	b)	Draw the block diagram of Control unit of a basic computer and explain its types.	[7M]

Or

6	a)	Show a possible control sequence for performing the operation MOV R1 R2.	[7M]
	b)	Elaborate on RISC.	[7M]

UNIT-IV

7	a)	What is Cache coherence problem? Explain various ways to resolve the Cache coherence problem.	[7M]
	b)	Explain about asynchronous data transfer and asynchronous communication interface.	[7M]

Or

8	a)	Explain in detail about Direct Memory Access in computer system.	[7M]
	b)	Distinguish between Programmed I/O and Interrupt driven I/O.	[7M]

UNIT-V

9	a)	Briefly discuss the types of Interconnection Structures.	[7M]
	b)	Explain about Serial and Parallel arbitration logic.	[7M]

Or

10	a)	Explain in detail the types of Parallel Processing.	[7M]
	b)	Define pipelining? Explain the structure of pipelining with an example.	[7M]
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