Code No: R2022022 **R20** **SET - 1**

II B. Tech II Semester Regular/Supplementary Examinations, July - 2023
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1 a) What are the characteristics of the 2's complement numbers? Explain with an example. [7M]
b) Derive the truth table of AND, OR and NOT gates with suitable diagrams. [7M]

Or

2 a) Convert the following binary number to Gray code and vice versa 110110 [7M]
b) Explain the duality principle with an example. [7M]

UNIT-II

3 a) Without reducing, convert the following expressions to NAND Logic [7M]
i) A+BC+ABC ii) (XY+Z) (XY+P)
b) Explain the function of Full Subtractor, supporting with truth table. [7M]

Or

4 a) Simplify the function of F=∑m (0,2,3,4,5,6) using K-Map. [7M]
b) Design a Half-adder logic diagram and explain it. [7M]

UNIT-III

5 a) Realize the logic expression F=∑m(0,1,3,5,8,11,12,14,15) using 8:1MUX. How many MUXs are required. [7M]
b) Draw a PAL circuit before and after implementation of a function F=ABC+BC+CA. Explain. [7M]

Or

6 a) Implement the logic expression F=∑m (0,2,4,7) using a 4:1 MUX, and 8:1 MUX. [7M]
b) Implement the following two Boolean functions with a PLA; [7M]
F_1(A,B,C)=∑m (0,1,2,4), F_2(A,B,C)=∑m (0,5,6,7)

UNIT-IV

7 a) What is the advantage and disadvantage of Ring counter compared to Ripple counter and explain the designing of a Ring counter? [7M]
b) Explain the operation of a JK FF and List out the applications $of\ \overline{PRESET}$. [7M]

Or

8 a) What are PRESET and CLEAR Inputs. Can a FF respond to its control and clock inputs while $\overline{PRE} = 1\ and\ \overline{CLEAR} = 1$. [7M]
b) How many states do a 4-bit i) Ripple counter ii) Ring Counter and iii)Jhonson counter have. Draw the states of any one of the counter. [7M]
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UNIT-V

9 a) Define and Draw the state table. What does each row, column and entry of the state table represent? [7M]

b) Obtain reduced state table and state diagram for the sequential machine whose state table is given below. [7M]

PS	N/S		O/P	
	X=0	X=1	X=0	X=1
a	c	b	1	1
b	d	c	0	0
c	(g)e	d	0	1
d	e	f	1	0
e	a	f	1	0
f	(g)e	f	1	0
g	a	f	1	0

Or

10 a) What is a transition table and output table? Explain with an example. [7M]

b) Design a JK-FF and describe Excitation Table, State Table and State diagram in Moore model. [7M]

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II B. Tech II Semester Regular/Supplementary Examinations, July - 2023

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UNIT-I

1	a)	Detect and correct errors, if any, in the even parity hamming codeword 1010111 and write the correct word.	[7M]
	b)	Explain the sign magnitude representation of numbers with suitable example.	[7M]

Or

2	a)	Explain about EVEN and ODD parity checking principle with suitable example.	[7M]
	b)	With suitable diagrams, explain the working of EX-OR gate, and EX-NOR gates. Write the other names.	[7M]

UNIT-II

3	a)	Obtain the real minimal expression for F=∑m (1,2,4,6,7) and implement it using Universal Gates.	[7M]
	b)	Realize Look-a-Head Carry adder.	[7M]

Or

4	a)	Reduce the expression F=∑m (1,5,6,12,13,14) + d(2,4) and implement the real minimal expression in Universal Logic.	[7M]
	b)	Design a Half-Subtractor and explain.	[7M]

UNIT-III

5	a)	Design a basic circuit of 1-bit magnitude comparator and explain.	[7M]
	b)	Tabulate the PLA programming table for the two Boolean functions listed below. i) A(x,y,z)= ∑m (0,1,6,7) ii) B(x,y,z)= ∑m (2,6)	[7M]

Or

6	a)	Explain the basic working principle of Encoder with help of block diagram.	[7M]
	b)	Prepare a truth table of 1-to-4 line De-Mux and draw the circuit diagram.	[7M]

UNIT-IV

7	a)	How do you convert one type of FF into another.	[7M]
	b)	Prepare excitation table for i) JK FF ii) D FF iii)SR FF	[7M]

Or

8	a)	Determine the number of FFs in each of the following counters. Mod3, Mod8, Mod14, Mod20, Mod32 and Mod150.	[7M]
	b)	Design and draw the timing diagram of Asynchronous 8-bit Upcounter using negative edge triggered FF.	[7M]
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UNIT-V

9 a) What is the Mealy model of the state diagram of a memory element. Give an example. [7M]

b) Draw an equivalent State diagram for the given state table in Moore Circuit modal and explain. [7M]

PS	$\frac{NS, O/P}{Input\ X}$		O/P
	X=0	X=1	
a	a	b	0
b	b	c	0
c	d	c	1
d	d	a	0

Or

10 a) Draw an equivalent State diagram for the given state table after in Moore Circuit modal and explain. [7M]

PS	N/S		O/P	
	X=0	X=1	X=0	X=1
a	b	d	0	1
b	e	f	0	1
c	b	d	0	1
d	e	b	0	1
e	e	f	0	1
f	f	c	0	0

b) Design a T-FF and describe Excitation Table, State Table and State diagram in Moore model. [7M]

Code No: R2022022 **R20** **SET - 3**

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Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
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UNIT-I

1	a)	Express the following 8421 BCD numbers as decimals: i) 0110 0111 1001 1000. 1000 and ii) 011010010111.0101	[7M]
	b)	Encode data bits 1101 into the 7-bit even parity Hamming code.	[7M]

Or

2	a)	Find the 10's complement of the following decimal numbers. i) 4069 ii) 1056.074	[7M]
	b)	Explain Demorgan Theorems with suitable example.	[7M]

UNIT-II

3	a)	Using the QUINE-MC CLUSKEY method of tabular reduction minimize the given combinational single output function F(w,x,y,z)= ∑m (0,1,5,7,8,10,14,15).	[7M]
	b)	Derive the functional equation of SUM and Carry of a Full-Adder?	[7M]

Or

4	a)	Using the tabular method , obtain the minimal expression for F= ∑m (6,7, 8,9)+d(10,11,12,13,14, 15)	[7M]
	b)	Derive the output functional equation of Half-Subtractor.	[7M]

UNIT-III

5		Design a BCD-to-Seven segment decoder with suitable minimization technique.	[14M]

Or

6	a)	Design a 3 line-to-3 line decoder with suitable example?	[7M]
	b)	Draw the internal logic of a 32 X 8 ROM and explain.	[7M]

UNIT-IV

7	a)	Implement a 3-bit ripple counter using D FFs.	[7M]
	b)	Design a RS Latch with NAND only and NOR only gates and compare the truth table.	[7M]

Or

8	a)	Define Race-around Condition? How can be eliminated this condition.	[7M]
	b)	Design a Jhonson Counter and explain the working with suitable waveforms.	[7M]
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UNIT-V

9 a) Obtain reduced state table and draw state diagram for the sequential machine whose state table is given below. [7M]

PS	N/S		O/P	
	X=0	X=1	X=0	X=1
a	A	B	0	0
b	c	b	0	1
c	d	a	1	1
d	c	b	0	1

b) Design a D-FF and describe Excitation Table, State Table and State diagram in Mealy model. [7M]

Or

10 a) Draw an equivalent State diagram for the given state table in Mealy Circuit modal and explain. [7M]

PS	$\frac{NS, O/P}{Input\ X}$	
	X=0	X=1
a	a,0	b ,0
b	b,1	c ,0
c	d,0	c ,1
d	d,0	a ,1

b) Design a SR-FF and describe Excitation Table, State Table and State diagram in Melaly model. [7M]

Code No: R2022022 **R20** **SET - 4**

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Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1	a)	Convert the Gray Code 1101 to Binary explain.	[7M]
	b)	List out Boolean theorems and explain any two with suitable example.	[7M]

Or

2	a)	Realize the XOR function using i) AOI Logic ii) NAND logic and iii) NOR Logic	[7M]
	b)	Explain about standard SOP and POS forms with suitable example.	[7M]

UNIT-II

3		Design an Ex-3 adder circuit with neat sketch and explain.	[14M]

Or

4		Draw a BCD adder circuit and explain the function.	[14M]

UNIT-III

5	a)	Realize the following functions using a PROM of size 8X3. I) F1(x,y,z)= ∑m (0,4,7), F2(x,y,z)= ∑m (1,3,6), F3(x,y,z)= ∑m (1,2,4,6),	[7M]
	b)	Design 1:16 MUX with 1:4 Mux. How many 1:4Muxs are required.	[7M]

Or

6	a)	How many OR gates are there in a 32x8RoM and how many inputs does each OR gate of a 32X8 ROM have.	[7M]
	b)	Explain the Principle of priority encoder.	[7M]

UNIT-IV

7	a)	Explain how to convert JK- Truth table into JK Excitation table. Explain.	[7M]
	b)	Classify the triggering techniques. Design 2-bit Ripple down counter using negative -edge triggered FF.	[7M]

Or

8	a)	Design a synchronous Counter using 3 JK FFs and explain with waveforms.	[7M]
	b)	Find the characteristic equation for a i) JK FF ii)D FF	[7M]

UNIT-V

9	a)	Compare the State diagram and the State table. Draw the suitable diagrams.	[7M]
	b)	Draw the state diagram and the State Table for a Moore type sequence detector to detect the sequence110.	[7M]

Or
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10 a) Draw an equivalent state diagram from the given State Table in Moore circuit modal. [7M]

PS	N/S		O/P
	X=0	X=1	
A	A	B	0
B	C	B	0
C	A	D	0
D	E	B	0
E	A	D	1

b) Design D-FF and describe Excitation Table, State Table and State diagram in Moore Model. [7M]