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Code No:R2022022 **R20** **SET - 1**

II B. Tech II Semester Regular Examinations, June/July - 2022

DIGITAL ELECTRONICS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit

All Questions carry **Equal** Marks

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UNIT-I

1 a) Convert the numbers $(0.3125)_{10}$ and $(1101.01)_2$ in base 8. [7M]

b) i. List the truth table of F = xy + xy' + y'z [7M]
ii. Draw logic diagrams to implement the Boolean expression
Y = A + B + B'(A +C')

Or

2 a) Subtract the two numbers using 10's complement and 9's complement 6,428 – 3,409 [7M]

b) Represent the decimal number 5.137 in (i) BCDcode (ii) Excess-3 code [7M]

UNIT-II

3 a) Simplify the following Boolean function, using three-variable maps: [7M]
$F(x, y,z) = \sum(0,2,6,7)$

b) Explain a four-bit binary adder circuit with relevant diagram. [7M]

Or

4 a) Why is a four-bit adder circuit implemented with full adders? Explain the designing procedure? [7M]

b) Draw a circuit for a two's complement implementer using the 4-bit adder cum subtractor circuit. [7M]

UNIT-III

5 a) Design a 8 to 1 digital multiplexer? Also design with 4:1 MUX? Explain? [7M]

b) Give the schematic circuit of a 2-to-4 binary decoder with an active-low enable input. Show theTruth Table. [7M]

Or

6 a) Show a multiplexer is also a Boolean expression implementer. [7M]

b) Draw a block diagram of a PLA and explain it's architecture. Write differences between PLA and PROM. What is the design procedure of a PLA based circuit? [7M]

UNIT-IV

7 a) Explain the designing procedure of Master Slave JK Flip-Flop with suitable diagram? [7M]

b) Draw the waveforms to enter a serial data 11101into a SIPO shift register. Explain? [7M]

Or

8 a) What is a decade counter? Explain its circuit and write the applications of a decade counter? [7M]

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b) What do we mean by SIPO, PISO, PIPO and SISO Shift registers? Explainwith timing diagram (i) shift left in each and (ii) shift right in each. [7M]

UNIT-V

9 a) Distinguish between a Transition table and Excitation table? Explain with an example. [7M]

b) Define Finite State machine for the state table using JK Flip-Flop. [7M]

Present state (Q_1Q_0)	Inputs (AB) 00	01	10	11
00	01	00	00	01
01	10	00	00	10
10	11	00	00	11
11	01	00	00	01
	Next State (Q_1^* Q_0^*)			

Or

10 a) What is the importance of reduction of number of states? What is the advantage of standard form for state tables? Explain with an example. [7M]

b) Explain the design procedure of Asynchronous sequential circuits. [7M]

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UNIT-I

1 a) Given the two binary numbers X = 10101111 and Y = 10000101, perform the subtraction (i) *X* - *Y* and (ii) *Y* - *X* by using 2's complement technique? [7M]

b) i. Express the Boolean function *F* = *xy*+ x'z as a product of maxterms [7M]
ii. Find the complement of F = wx + yz; then show that FF' = 0 and F+ F' = 1

Or

2 a) Convert the following expressions into sum of products and product of sums: [7M]
i. (AB + C'D)(B+C'D)
ii. X' + x(x + y')(y + z')

b) Draw the logic diagram to the following Boolean expressions without simplifying them: [7M]
i. BC'+AB+ACD
ii. (A+B)(C+D)(A'+B+D)

UNIT-II

3 a) Simplify the following Boolean function, using three-variable maps: [7M]
$F(x, y,z) = \sum (0,2.3,4,6)$

b) Draw the circuit diagram of a 2-bit adder-subtractor and explain the function? [7M]

Or

4 a) Draw the block diagram of a full adder using two half adders and one OR gate. [7M]

b) Simplify the following Boolean expression, using three-variable maps: [7M]
F(x,y,z) = xy + xy'z' + x'yz'

UNIT-III

5 a) Design a combinational circuit that will accomplish the multiplication of the 2-bit binary numberX_1 X_0 by the 2-bit binary number Y_1 Y_0. Is a two-level circuit the most economical? Justify? [7M]

b) What is advantage of a PROM compared to the PLA and PALs? Explain. [7M]

Or

6 a) Construct a 4 X16 decoder using five 2 X4 decoder modules. Explain with a neat schematic diagram. [7M]

b) What is the difference between a digital multiplexer and a digital demultiplexer? Explain with an example? [7M]

UNIT-IV

7 a) Define D and T flip-flop with the help of truth table? Also design the D and T flip-flop using JK flip flop? [7M]

b) Design a 4-bit asynchronous decade counter and draw the timing diagram. [7M]

Or
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8 a) Draw the timing diagram of a 4-bit asynchronous counter and explain? [7M]

b) Draw and explain briefly an Asynchronous Mod-12 counter? [7M]

UNIT-V

9 a) Design a 5 state sequential machine whose sequential states are: 000, 001, 010, 110, 111, 000…..Assume initial state is 000. [7M]

b) Explain the design procedure of synchronous sequential circuits. [7M]

Or

10 a) Why state reduction is necessary in sequential circuit design? What are the different methods of state reduction? Explain implication table method of state reduction with an example. [7M]

b) A synchronous counter is controlled by two input signals A and B. The counter does not operate, ifA = 0 and B = 0. When A = 0 and B = 1, the counter operates as a mod four counter. If A=1 and B=0 the counter operates as a mod eight counter. Draw an FSM chart and design a circuit? [7M]

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UNIT-I

1 a) i. Subtract $(12.50)_{10}$ from $(18.75)_{10}$ in binary using 1's complement method? [7M]
ii. Find the Gray Code number for the given 12-bit binary number
1 0 0 1 1 0 1 0 0 1 1 1 and explain the procedure?
b) Implement the Boolean function F = xy + x'y' + y'z with AND, OR and inverter gates [7M]

Or

2 a) Express the following sum-of -Products function F(A,B,C,D) = Σ(3,5,9,11,15) in to POS form. [7M]
b) Show that the dual of the exclusive-OR is equal to its complement? [7M]

UNIT-II

3 a) Simplify the following Boolean expression, using any two mapping techniques. [7M]
F(x,y,z) = xy + x'y'z' + x'yz'
b) Implement 8-bit adder circuit using full adders as the building blocks. [7M]

Or

4 a) Simplify the Boolean function, F(A,B,C,D)=∑(0,1,4,5,7,15)+d(10,11, 14). Explain the procedure? [7M]
b) Draw the logic diagram of a half subtractor using NOR gates only. [7M]

UNIT-III

5 a) Implement the following function using a multiplexer of proper size.F(w, x, y, z) = ∑m(0, 1, 2, 3, 4, 9, 13, 14, 15) [7M]
b) Give the logic circuit schematic to realize a BCD to decimal decoder. [7M]

Or

6 a) Design a 4 bit comparator using PROMs? [7M]
b) What is a difference between an encoder and a decoder? Explain with an example. [7M]

UNIT-IV

7 a) What are the differences in a Master Slave JK FF, a Positive edge triggered JK-FF and a Negative edge triggered JK-FF? [7M]
b) Draw a logic diagram of 4-bit ripple counter and explain its operation with timing diagram and sequence table. What modification is required to use as a decade counter? [7M]

Or

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8 a) Write the difference between the following counters [7M]
(a) Synchronous counter and asynchronous counter
(b) Binary UP and binary DOWN counter

b) Draw the logic circuit diagram of universal shift register and explain its operation with functional table. [7M]

UNIT-V

9 a) Write design procedure of a finite state machine. [7M]

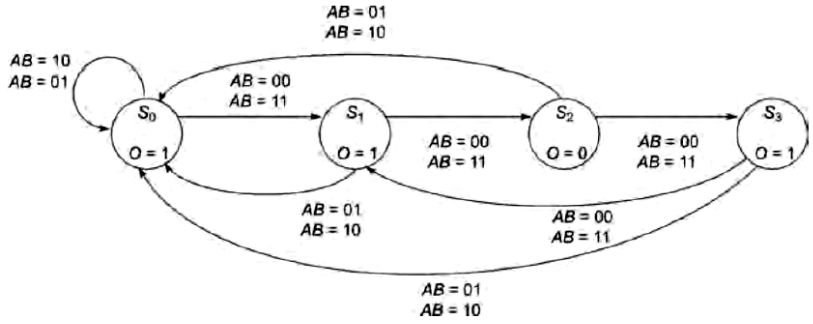
b) Design a sequential circuit (finite state machine) for Table given below using D flip-flops.Assume two inputs are A and B, outputs of the sequential circuit are outputs of Dflip-flops, present state =S, Next State=S*. Consider the four states of the sequentialcircuit are S_0=00, S_1=01, S_2=10 and S_3=11. [7M]

	Inputs (*AB*)			
Present state (*S*)	**00**	**01**	**10**	**11**
S_0	S_1	S_0	S_0	S_1
S_1	S_2	S_0	S_0	S_2
S_2	S_3	S_0	S_0	S_3
S_3	S_1	S_0	S_0	S_1
	Next State (S^*)			

Or

10 a) Draw the state diagram and state table of a up-down counter. Design the Up-Down counter using Tflip-flops. [7M]

b) The state diagram of a sequential circuit is given in Fig. Draw the state table for Fig. Assume two inputs are A and B, output is O. [7M]



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UNIT-I

1 a) Generate a Hamming Code for the given 4-bit message word 1001 and rewrite the entire message in Hamming Code. [7M]
b) Obtain the truth table of the function, and express function in sum-of-minterms and product of max terms Y (xy + z)(y + xz). [7M]

Or

2 a) For the Function F = xy'z+ x'y'z + w'xy+ wx'y+ wxy, draw the logic diagram using original Boolean expression and also for simplified expression. Compare the total number of gates for the two. [7M]
b) Convert the given number "B2FA" to binary and Find the 2's complement of the result? [7M]

UNIT-II

3 a) Simplify the Boolean function, using five-variable maps [7M]
F(A,B,C,D,E)=A'B'CE'+B'C'D'E'+A'B'D'+B'CD'+A'CD+A'BD
b) Design a full-subtractor circuit with three inputs x,y, B_{in} and two outputs *Diff* and B_{out}. Where B_{in} is the input borrow, B_{out} is the output borrow and *Diff* is the difference. [7M]

Or

4 a) Draw a logic diagram using only two-input NOR gates to implement the following function: F(A,B,C,D) = (A⊕B)'(C⊕D) [7M]
b) Design the Excess-3 code adder circuit. [7M]

UNIT-III

5 a) Implement the following logic function with 2n X1 multiplexer, where n is the number of variables in the function. F(A, B, C, D) = S(4, 5, 6, 7, 8, 13, 14, 15). [7M]
b) Why does a carry look-a-head generator give a fast adder? How much is the speed up for an 8-stage circuit? Explain. [7M]

Or

6 a) What is a difference between a decoder and a digital demultiplexer? Explain their truth table differences by taking an example. [7M]
b) Construct a 4 X16 decoder using two 3 X 8 decoder modules and additional logic. Show the schematic diagram neatly. [7M]

UNIT-IV

7 a) How does a SR latch differ from a gated RS latch? [7M]
b) Write the count sequence of 3-bit binary ripple counter. Design a 3-bit ripple counter using J-K flip-flops [7M]

Or

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8 a) Design a 4-bit binary UP/DOWN ripple counter with a control input for UP/DOWN counting [7M]

b) Design a PIPO, which is a 4-bit buffer register with parallel in (loading) and parallel output (storing) [7M]

UNIT-V

9 a) Write difference between Mealy and Moore machines in detail. [7M]

b) Design a sequential circuit for the state Table using D flip-flops. Assume twoinputs are A and B, output of the sequential circuit is O, present state of D flip-flops = Q_1Q_0, Next State of D flip-flops = (Q_1* Q_0*). [7M]

	Inputs (*AB*)			
Present state(Q_1Q_0)	**00**	**01**	**10**	**11**
00	01/0	00/0	00/0	01/0
01	10/1	00/1	00/1	10/1
10	11/0	00/0	00/0	11/0
11	01/1	00/1	00/1	01/1
	Next State (Q_1* Q_0*)/Output(O)			

Or

10 a) A sequential circuit has two inputs X and CLOCK and one output O. Incoming data are examined in consecutive groups of three digits and the output O=1 for the following three input sequences 000, 010 and 111. Draw a state diagram and implement the sequential circuit using J-K flip-flops. [7M]

b) Define Finite state machine for the state table using D Flip-Flops. [7M]

	Inputs (*AB*)			
Present state (Q_1Q_0)	**00**	**01**	**10**	**11**
00	01	00	00	01
01	10	00	00	10
10	11	00	00	11
11	01	00	00	01
	Next State (Q_1* Q_0*)			