Code No: R2022042 **R20** **SET - 1**

II B. Tech II Semester Regular Examinations, June/July - 2022

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1 a) Explain the various Data Objects supported by VHDL. Give the necessary examples? [7M]

b) Define the following terms relevant to Verilog HDL [7M]
i) Parameters iii) Constants
ii) Keywords iv) identifiers

Or

2 a) Explain the difference in program structure of VHDL and any other procedural language. Give an example. [7M]

b) What is the use of library clause and use clause? Give example. [7M]

UNIT-II

3 a) Design a 4-bit carry look ahead adder using gates and write data flow VHDL program. [7M]

b) Design a 3-bit comparator using three one bit comparators and logic gates. [7M]

Or

4 a) What is multiplexer? Draw the logic diagram of 8 to 1 line multiplexer? [7M]

b) Design a 32 to 1 MUX using 74x151 and 74x139 decoders. [7M]

UNIT-III

5 a) Design and Explain the operation of 4-bit ring counter with the help of an IC? [7M]

b) Implement the verilog HDL module of N-bit Synchronous Up/Down counter? [7M]

Or

6 a) Design and Explain a 4-bit Ripple counter with the help of an IC? [7M]

b) With suitable logic diagram explain a 4-bit bidirectional shift register? Also write the VHDL source code for the same? [7M]

UNIT-IV

7 a) Design a 3-input CMOS OR-AND-INVERTER gate. Draw the logic diagram and function table. [7M]

b) Discuss a Pseudo-NMOS logic and design XNOR gate using it? [7M]

Or

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8 a) Draw a circuit diagram, functional table, and logic symbol for a CMOS gate with two inputs A and B and an output Z where Z=1 if A=0 and B=1, and Z=0 otherwise. [7M]

b) What is a Complementary Pass-Transistor Logic (CPL)? Draw the Circuit diagram of CPL NAND2 gate and CPL NOR2 gate. [7M]

UNIT-V

9 a) Construct a Gate-level schematic of the clocked NAND-based JK latch circuit and explain its operation with detailed truth table? [7M]

b) Design Schmitt trigger using CMOS and explain its operation? [7M]

Or

10 a) Design CMOS SR latch circuit based on NOR2 gates and explain its operation with the help of truth table? [7M]

b) Draw different styles of D-FlipFlops using CMOS and transmission gates and explain any one? [7M]

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Answer any **FIVE** Questions each Question from each unit
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UNIT-I

1 a) Explain various architectural bodies/modeling styles in VHDL with examples. [7M]
b) Explain the various data types supported by VHDL. Give the necessary examples. [7M]

Or

2 a) Write the differences between Verilog and VHDL? Write the Syntax of CASE INVERTOR? [7M]
b) Write a Verilog code for a 4X1 MUX using CASE statement? [7M]

UNIT-II

3 a) Design a 2 input 4-bit multiplexer. Write the truth table and draw the logic diagram. [7M]
b) Using a process statement write a VHDL source code for 4 to 1 multiplexer. [7M]

Or

4 a) Draw the logic diagram of 74x283 IC and design a 24-bit ripple adder using the same IC. [7M]
b) Write a VHDL code for four bit parallel adder/subtractor. [7M]

UNIT-III

5 a) Draw the circuit diagram of a 4-bit binary counter and explain its working with its function table and write its Verilog code? [12M]
b) Tabulate the comparisons between synchronous sequential and asynchronous sequential circuits. [2M]

Or

6 a) List the basic types of shift registers in terms of data movement with diagrams? [2M]
b) Write a verilog description of the 8-bit parallel in/parallel out shift register for multiplication and division operations and write its test bench? [12M]

UNIT-IV

7 a) Draw a circuit diagram, functional table, and logic symbol for a two input depletion-load NOR gate and explain its functional behavior. [7M]
b) Define threshold voltage of a MOS device and explain its significance. [7M]

Or

8 a) What is a CMOS transmission gate? Implement Ex-OR and Ex-NOR Boolean functions using transmission gate. [7M]
b) Design an area efficient layout diagram for the CMOS logic shown below [7M]
$Y = (A + B + C)^{1}$

UNIT-V

9 a) Draw the Gate-level schematic and block diagram of the NAND-based SR latch and explain the operation with the help of function table. [7M]
b) List out the comparisons between latch and flip flop. [7M]

Or

10 a) Design and Explain the operation of CMOS clocked JK flip-flop [12M]
b) List out the differences between regenerative logic circuits and non-regenerative logic circuits. [2M]

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Code No: R2022042 **R20** **SET - 3**

II B. Tech II Semester Regular Examinations, June/July - 2022

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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UNIT-I

1 a) Explain the program structure of VHDL with the help of block diagram. [7M]
b) With suitable examples explain the various data types supported by VHDL. [7M]

Or

2 a) List out the different Operators available in Verilog HDL. Explain with example. [7M]
b) What are the various data types supported by Verilog HDL? Explain about the predefined data values used for net or variable data type? [7M]

UNIT-II

3 a) Design the logic circuit for even parity checker and write the behavioral VHDL program? [7M]
b) What is a comparator? Explain the operation of a 2-bit comparator with a relevant diagram. Draw its logic symbol and write a VHDL code. [7M]

Or

4 a) Design the following code converters: [7M]
i) 5211 to 2421 ii) 4-bit binary to excess-3
b) Design a first and second highest priority encoder circuit using 74LS148 and 74LS138? [7M]

UNIT-III

5 a) Draw the logic diagram for n-bit left to right shift register? Write down the VHDL code for an n-bit left to right shift register? [9M]
b) List out the applications of shift register? [5M]

Or

6 a) Discuss the logic circuit of 74 x 377 register. Write a VHDL program for the same in structural style. [9M]
b) Give brief note on hazards in sequential circuits? [5M]

UNIT-IV

7 a) Design a CMOS transistor circuit for 2-input NAND gate. With the help of function table explain the circuit. [7M]
b) With suitable example, discuss about the requirement and operation of pass transistors and design AND gate using it? [7M]

Or

8 a) Draw the circuit diagram of two-input depletion-load NOR gate and calculate the output low and output high voltages for the same? [7M]
b) Design and Explain CMOS full-adder circuit? [7M]

UNIT-V

9 a) Draw the logic diagram and truth table of a CMOS clocked SR flip-flop and explain its operation? [7M]
b) With neat schematic explain D latch using CMOS Inverter and Transmission gate? [7M]

Or

10 a) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation? [7M]
b) Design Schmitt trigger using CMOS and explain? [7M]
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DIGITAL IC DESIGN

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Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1	a)	Explain the different concurrent statements and sequential statements in VHDL?	[7M]
	b)	Discuss about the comparison between CASE and IF statements in VHDL with examples?	[7M]

Or

2	a)	Give the syntax for a net declaration? Explain the different kind of nets that belong to the net data type?	[7M]
	b)	How the package declaration is different from entity declaration? Give the syntax for each?	[7M]

UNIT-II

3	a)	Draw the logic symbol and logic diagram of 74 X 148 priority encoder. Give its truth table and write VHDL code in any one of the model.	[7M]
	b)	Explain the design procedure for multiplexers and de-multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates.	[7M]

Or

4	a)	Give circuit implementation of 4 Bit Ripple adder and Ripple Adder/Subtractor using ones and twos complement method.	[7M]
	b)	Design a Binary to Gray Code converter and write its VHDL code using data flow modeling ?	[7M]

UNIT-III

5	a)	List the basic types of shift registers in terms of data movement with diagrams?	[2M]
	b)	Design & explain 4-bit serial-In Parallel-out register and write its VHDL code?	[12M]

Or

6	a)	Explain the operation of a 4 bit synchronous binary counter with the required diagram and waveforms.	[7M]
	b)	Design a 4-bit binary synchronous counter using 74x74 IC. Write the VHDL source code for the same.	[7M]

UNIT-IV

7	a)	Draw the generalized NOR structure with multiple inputs using Pseudo nMOS and explain the operation with the help of functional table?	[7M]
	b)	Develop complementary Pass-transistor logic? Design OR operation using Pass-transistor logic?	[7M]

Or
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8 a) Draw and explain the CMOS Half adder? [7M]

b) How does a transmission gate work? Explain four different representations of the CMOS transmission gate (TG). Design 2X1 MUX using it? [7M]

UNIT-V

9 a) Explain the operation of a D-latch using CMOS through suitable timing diagram for various possibilities of input. [7M]

b) Design CMOS JK Flip flop and explain? [7M]

Or

10 a) With the help of neat circuit diagram explain the operation of a CMOS bistable element? [7M]

b) Design D-Flip flop using CMOS Inverter and transmission gates as switches? [7M]