Code No: R2031041 **R20** SET - 1

III B. Tech I Semester Supplementary Examinations, May/June -2024
ANALOG ICS AND APPLICATIONS
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) What is slew rate? Analyze the causes of slew rate and explain its significance in applications. [7M]
   b) Draw the functional diagram of LM78XX series fixed voltage regulator and describe its operation. [7M]

(OR)

2. a) Explain the functions of all the basic building blocks of an op-amp with a neat diagram. [7M]
   b) What is the principle of switched mode power supplies? Discuss its merits and demerits. [7M]

UNIT-II

3. a) Design a differentiator using op-amp to differentiate an input signal with 1 kHz. Draw the equivalent circuit. [7M]
   b) Draw the circuit diagram of a logarithmic amplifier using op-amps and explain its operation. [7M]

(OR)

4. a) Draw the circuit of a voltage to current converter if the load is (i) floating, and (ii) grounded. Is there any limitation on the size of the load when grounded? [7M]
   b) Explain the operation of a practical sample-and-hold circuit with a neat diagram. What are its applications? [7M]

UNIT-III

5. a) Design a second-order Butterworth High pass filter with cut-off frequency of 10 kHz, given that $2K_1 = 0.765$ and $2K_2 = 1.848$. [7M]
   b) Design a wideband bandpass filter with $f_L = 200$ Hz and $f_H = 1$ kHz and calculate the value of Q for the filter. [7M]

(OR)

6. a) Design a second order Butterworth high-pass active filter with the following specifications with the circuit configuration:
   (i) Voltage gain = 2.5
   (ii) Cut-off frequency = 5 kHz. [7M]
   b) Given a bandpass filter with lower and higher cut-off frequencies of 50 Hz and 60 Hz respectively, find its(i) quality factor, (ii) resonant frequency, and (iii) bandwidth. [7M]

UNIT-IV

7. a) Design an astable multivibrator to get output wave form at 10 kHz, with a duty cycle of 75% using 555 IC. [7M]
   b) Discuss the application of PLL IC for frequency multiplication. Differentiate between frequency multiplication and frequency translation. [7M]

(OR)

8. a) Give the pin configuration of 555 IC and explain its working. [7M]
   b) Using neat sketches, explain how a PLL can be used as frequency translator. [7M]

UNIT-V

9. a) Explain the principle and operation of simultaneous-conversion type analog to digital converter. [7M]
   b) How many bits are required to design a digital to analog converter that can have a resolution of 5 mV? The ladder has +8V full scale. [7M]

(OR)

10. a) Draw the necessary waveforms and explain the working principle of a dual-slope integrating type ADC. Describe the necessary expression for accumulated counts. [7M]
    b) For a 4-bit R–2R ladder digital to analog converter assume that the full-scale voltage is 10 V. Calculate the step change in output voltage when the input changes from 1001 to 1110. [7M]