Code No: R203105K **R20** SET - 1

III B. Tech I Semester Supplementary Examinations, July -2023
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to EEE,ECE**)**

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1.	a)	Make use of Arithmetic to perform $(356)_{10}$ to $(\ )_2$,$(\ )_4$,$(\ )_8$,$(\ )_{16}$ & BCD conversions.	[7M]
	b)	Perform the following using BCD Arithmetic (8129)10+(8811)10.	[7M]
		(OR)	
2.	a)	Develop AND and OR gates using NAND gates.	[7M]
	b)	Simplify the following Boolean function in POS form using K-map F(A.B.C,D)=$\pi M(4,6,10,12,13,15)$	[7M]

UNIT-II

3.	a)	Implement full adder and full Subtractor using Half adders and Half Subtractor.	[7M]
	b)	Model the 3 X 8 Decoder using 2X4 Decoder	[7M]
		(OR)	
4.	a)	Construct D Flip Flop by using SR Flip Flop.	[7M]
	b)	Explain the operation of JK Flip Flop. What is race around condition and suggest a remedy for it.	[7M]

UNIT-III

5.	a)	Discuss the Basic Functional Units of a Computer?	[7M]
	b)	Explain about the Bus structures of computer?	[7M]
		(OR)	
6.	a)	Write short notes on arithmetic and logic micro operations?	[7M]
	b)	Discuss about the basic instruction types of a computer?	[7M]

UNIT-IV

7.	a)	Explain the concept of the control memory?	[7M]
	b)	Draw and Explain the micro programmed control unit?	[7M]
		(OR)	
8.	a)	Define the Instruction formats? Explain the types of instruction formats with any examples?	[7M]
	b)	Explain briefly program control unit?	[7M]

UNIT-V

9.	a)	Define the Cache memory? Explain any two mapping techniques of cache memory.	[7M]
	b)	Discuss about the Auxiliary memory?	[7M]
		(OR)	
10.	a)	Explain the DMA Architecture?	[7M]
	b)	Discuss the Asynchronous data transfer modes?	[7M]