Code No: R203104Q **R20** SET - 1

III B. Tech I Semester Supplementary Examinations, July -2023
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) i) Convert $(8B7.A4)_{16}$ toits binary equivalent. [7M]
   ii) Convert $(714.36)_8$ to its hexadecimal equivalent.
   b) Encode the binary word 10111 into 9 bit hamming code for odd parity. [7M]

(OR)

2. a) i) What are the universal gates? Why they are called as universal gates? Discuss with the figures. [7M]
   ii) Draw the Logic diagram and explain the truth table of EX-OR and EX-NOR gates.
   b) i) State and prove De-morgan theorems. [7M]
   ii) Reduce the following Boolean Expression:
   AB+ABC+AB(D+E).

UNIT-II

3. a) Simplify the following function using K-Map: [7M]
   $F(A,B,C,D)=\sum(0,2,3,8,10,11,12,14)$
   b) Design a full adder by using two half adders. [7M]

(OR)

4. a) Simplify the following function using K-Map: [7M]
   $F(A,B,C,D,E)= \Pi(0,1,6,7,8,9,21,22,23,29,31)$
   b) Implement Carry look-a-head adder circuit and explain its operation briefly. [7M]

UNIT-III

5. a) Implement the following Boolean functions using PROM: [7M]
   $F_1(A_2,A_1,A_0)=\sum(0,1,2)$, $F_2(A_2,A_1,A_0)=\sum(3,4,5)$, $F_3(A_2,A_1,A_0)=\sum(2,4,6)$
   b) Draw the pin diagram and obtain the truth table of IC 7485? [7M]

(OR)

6. a) Design a 4 to 2 priority encoder. [7M]
   b) Implement the following Boolean function using 4:1 Mux: [7M]
   $F(A,B,C,D)=\sum(0,2,3,6,11,13,15)$

UNIT-IV

7. a) What is a Flip flop? Explain the SR flip flop with the help of logic diagram, truth table and excitation table. [7M]
   b) Design a 3 bit Synchronous Counter. [7M]

(OR)

8. a) Convert SR Flip flop into JK flip flop. [7M]
   b) What is a register? Explain the operation of Parallel In Serial Out shift register (PISO). [7M]

UNIT-V

9.	a)	Explain the differences between Mealy and Moore Machine.	[7M]
	b)	What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine.	[7M]
		(OR)	
10.	a)	Explain the designing steps to convert Mealy machine to Moore machine.	[7M]
	b)	Design a finite state machine which can detect the sequence 0010.	[7M]